Semiconductor and beyond

Global semiconductor industry outlook 2026

Agenda

1 Foreword

2 Demand Analysis

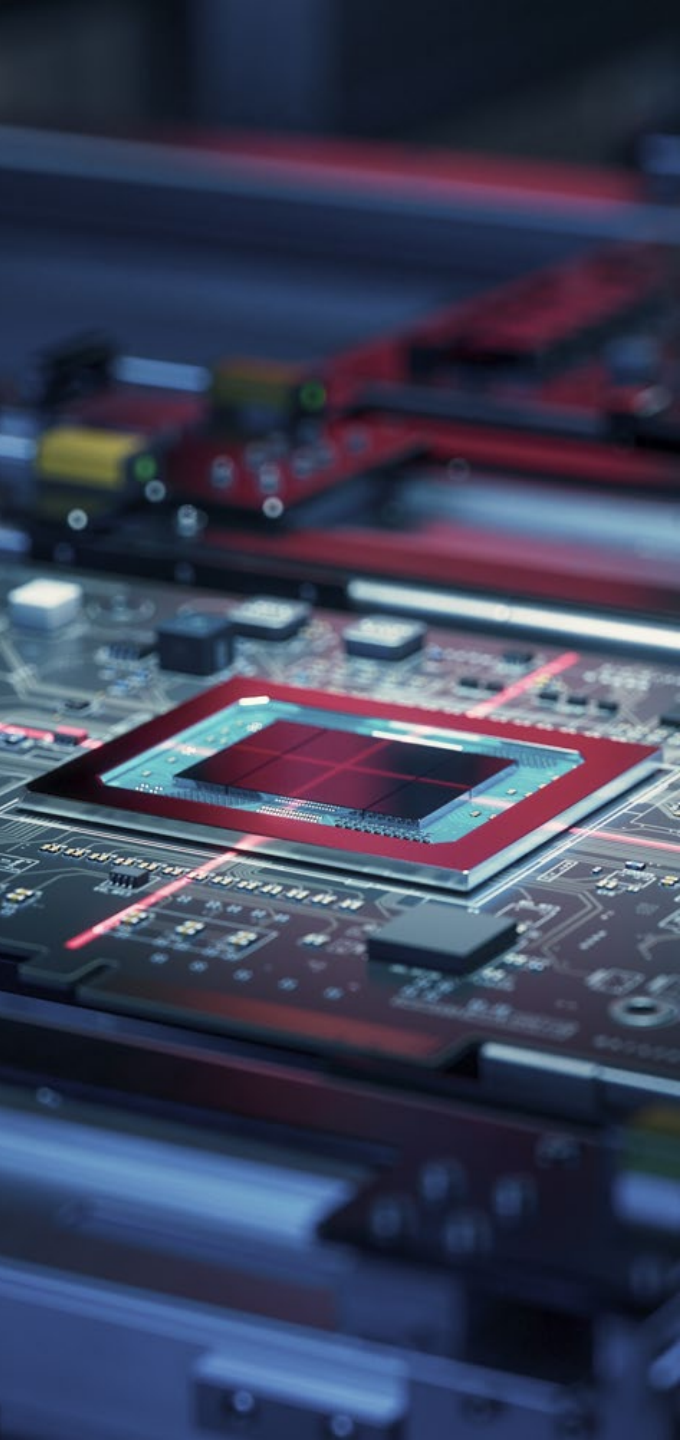
Semiconductors power innovation and everyday life

3 Supply Analysis

The race for semiconductor supremacy

4 What’s Next?

Opportunities in semiconductor : AI and beyond



Foreword

The semiconductor industry is undergoing rapid transformation, shaped by AI advancements, geopolitical shifts, and increased government investments in domestic production. As AI adoption accelerates, demand for high-performance chips is surging, while supply chain dynamics are being reshaped by evolving trade policies and national security concerns. At the same time, semiconductors are becoming indispensable across industries such as automotive, healthcare, and energy, driving the need for continuous innovation and strategic adaptation. Supply chain resilience and technology sovereignty are now top priorities for both businesses and governments. Efforts to diversify production and reduce dependencies are underway, yet structural challenges remain. Export controls, restrictions on critical materials, and shifting trade alliances are redefining the semiconductor landscape, requiring companies to navigate increasing complexity while maintaining their competitive edge.

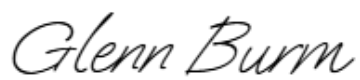
At PwC, we have worked alongside semiconductor leaders through multiple industry shifts, helping clients adapt to evolving market conditions, enhance supply chains and drive long-term sustainable growth.

Our deep industry expertise enables us to provide strategic insights on supply chain restructuring, operational efficiency, and technology innovation. As the competitive and regulatory landscape continues to evolve, we remain committed to helping businesses mitigate risks, identify growth opportunities, and position themselves for long-term success. As semiconductors become even more central to global innovation and economic security, companies must take a forward-looking approach to remain competitive. Through this report, we aim to provide industry leaders, policymakers, and businesses with the insights they need to navigate the future of this dynamic sector. PwC stands ready to support organizations in addressing challenges, seizing opportunities, and unlocking the potential of the semiconductor industry.

Glenn Burm

Partner

Global Semiconductors Leader



Semiconductor and beyond

Key highlights

PwC's 'Semiconductor and beyond' offers a strategic perspective on the global semiconductor industry and is structured into three parts: "Demand analysis", which conducts market demand study based on five end-markets, "Supply analysis", which explores the dynamics of each value-chain, and the "What's next?", which provides strategic forecasts regarding future technologies.

Looking ahead, in the "Demand analysis", the semiconductor market is projected to grow from $0.6 trillion in 2024 at a compound annual growth rate (CAGR) of 8.6%, surpassing $1 trillion by 2030. Among the various sectors, semiconductors for Server and Network are expected to grow the fastest, at an annual rate of 11.6%, driven by the rapid increase in generative AI services. The second-fastest growing sector is Automotive, anticipated to grow at an annual rate of 10.7%, propelled by advancements in electric vehicles and autonomous driving technologies. Through this analysis, we explore the role of semiconductors in five major sectors, shifts in demand patterns, and the broader impacts shaping the industry. Additionally, we analyze how technological advancements influence semiconductor consumption and development.

Next, on the "Supply analysis", technology development and investment are concentrated on expanding capacity and advancing processes around leading nodes. Although the progression of these nodes is vital to the industry, the competitiveness of supply chains varies from territory to territory. Historically, the United States has had a strong foothold in chip design, while Asia has excelled in fabrication. On the other hand, Southeast Asian regions are at the forefront of developing packaging technologies. However, evolving demand, technological challenges, and geopolitical shifts are reshaping the semiconductor supply chain, likely triggering significant disruptions.

Lastly, the 'What's Next?' section offers a long-term analysis of innovative technologies set to significantly influence the semiconductor market beyond 2030. Among many innovative advancements, we evaluate the technology feasibility and market potential of these technologies with quantitative insights. Recognizing these enduring and interconnected trends, we analyze the technologies, uncertainties, and key questions they raise. This analysis can offer vital insights for market entrants and policy makers on the future dynamics of the semiconductor industry.

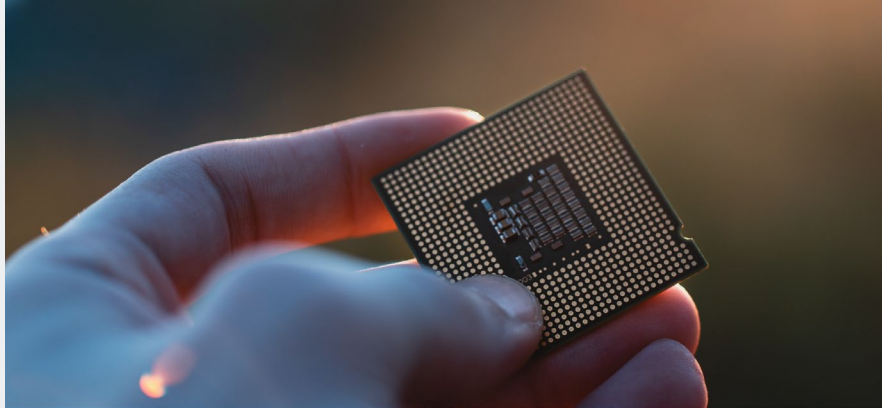
2

Demand Analysis

Semiconductors power innovation and everyday life

Why demand matters?

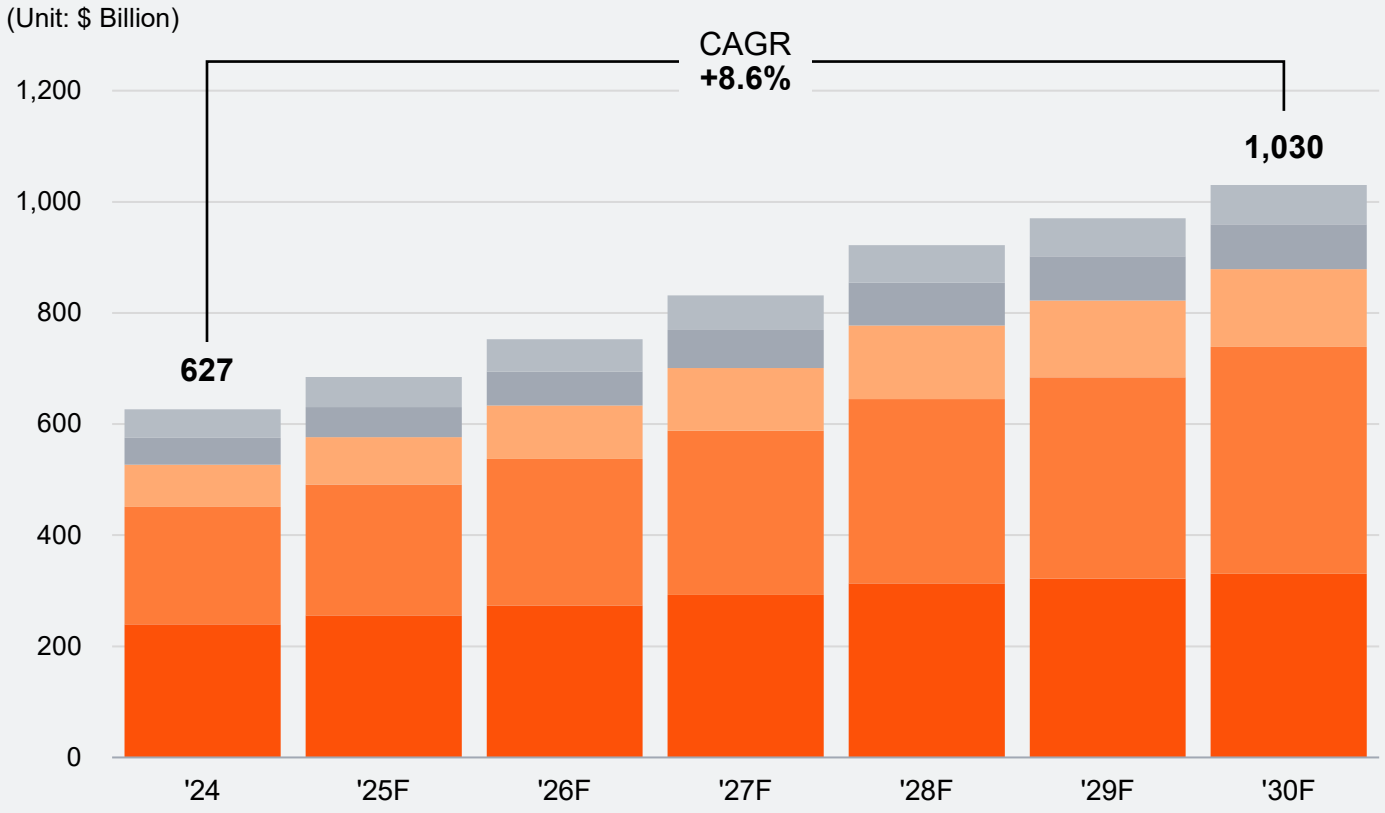
Semiconductors are indispensable in today's world, driving strong, evolving market demand due to rapid technology advancements and rising sector needs. As demand outpaces supply, analyzing these dynamics can reveal diverse pathways to seize emerging opportunities.



End-market	**Automotive** · **Server and Network** · **Home Appliances** · **Computing Devices** · **Industrial**
End-market dynamics	Analyze end-market dynamics to help predict the future of the semiconductor market since semiconductors are significantly influenced by the end-market dynamics
Semiconductor trends	Analyze the recent rapidly changing demand trends related to the application or focus on major semiconductor chips to analyze the key trends in the market
Demand outlook	Analyze the semiconductor market demand by application, the growth rate of each market, and the change in the proportion of semiconductors as part of the total cost to assess the demand intensity for semiconductors by 2030

Global semiconductor demand by end-market

As a backbone and enabler of data centers, AI, autonomous vehicles, smartphone and further emerging technological trends, the global semiconductor market is projected to grow from $627B (2024) to $1,030B (2030F), driven by widespread advancements across end markets.



End-market	CAGR[1] ('24-'30F)
Home Appliances	+5.6%
Industrial	+8.8%
Automotive	+10.7%
Server and Network	+11.6%
Computing Devices	+5.5%

1) Compound Annual Growth Rate
Source: Omdia, PwC analysis

Automotive

The automotive industry is undergoing a profound transformation driven by electrification, autonomous driving, and software-defined vehicles (SDVs). These trends are rapidly becoming the industry standard, amplifying the role and value of semiconductors in modern vehicles.

As the electric vehicle (EV) market is expected to take the majority share around 2030, demand for high-voltage power semiconductors like silicon carbide (SiC) is set to surge. At the same time, autonomous driving technology may advance, with most vehicles reaching level 2 and an increasing number achieving level 3. This evolution can drive up the semiconductor content per vehicle, ranging from sensors and connectivity integrated circuits (ICs) to processing units. The rise of SDVs may move vehicles toward a zonal architecture with centralized computing power, raising the performance requirements of automotive systems-on-chip (SoCs).

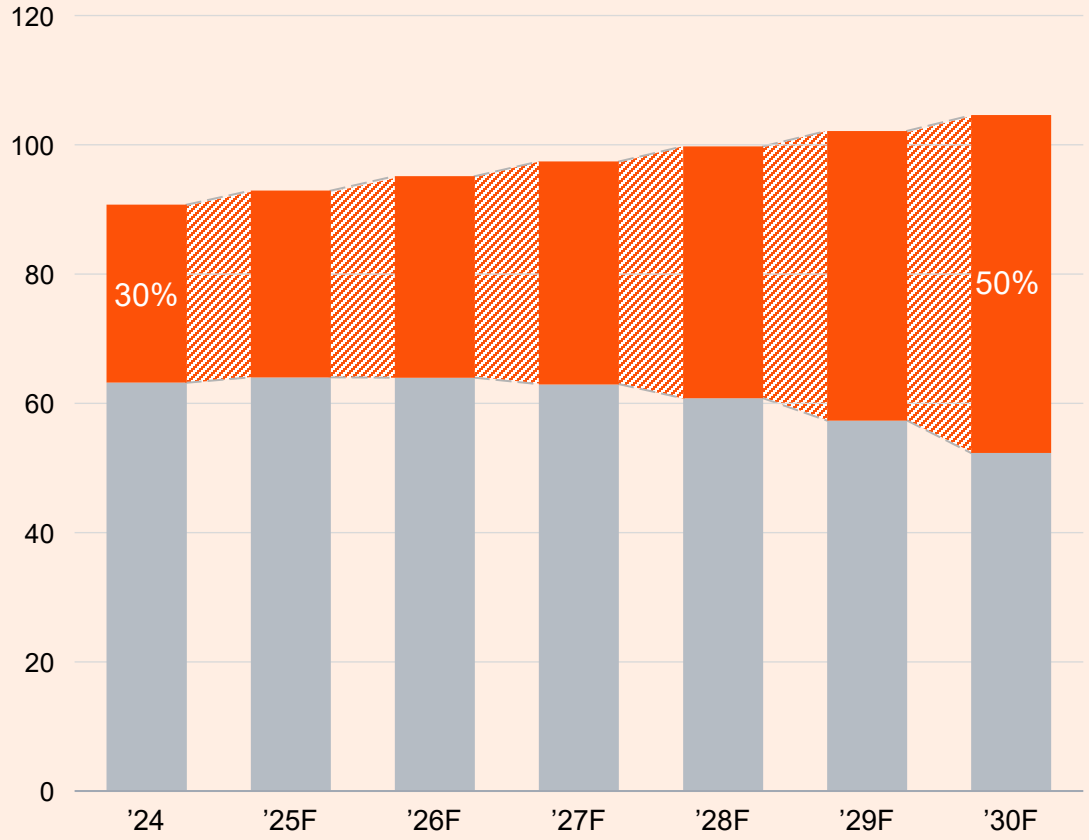
The car of the future may be more than just a mode of transportation – it can be a new form of home, a high-performance computer on wheels, seamlessly powered by semiconductors.

Electrification and connectivity

The automotive industry is currently undergoing a transformative phase marked by electrification, autonomous driving, and connectivity. With the EV market rapidly expanding, first by China and soon Europe, the US, and other regions, original equipment manufacturers (OEMs) are increasingly investing in hybrid and EVs. It is anticipated that these vehicles might account for around 50% of the total vehicle sales by 2030.

The emergence of connected and self-driving cars is also shaping the future of the automotive market, driving its maturation. These trends, combined with the shift in powertrain technology, can become the new standard for the automotive industry, elevating the role of semiconductors.

Global automotive sales (Unit: Million)



CAGR, 2024-30F	
Electric Vehicle[1)]	11.3%
Internal Combustion Engine	-3.1%

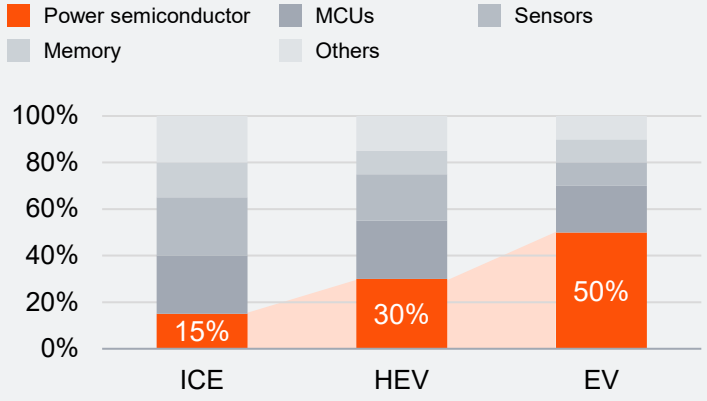
1) Electric Vehicle includes Battery Electric Vehicle, Hybrid Electric Vehicle and Plug-in Hybrid Electric Vehicle.
Source: PwC Autofacts, PwC analysis

More EVs? More power!

The rapid growth of EVs, along with the integration of infotainment and autonomous driving, is increasing the demand for power semiconductors. These are essential for managing and converting the electrical systems within modern vehicles.

As the automotive industry transitions from internal combustion engine (ICE) to hybrid EVs (HEVs) and EVs, power semiconductors may account for more than 50% of the total semiconductor cost.

Semiconductor cost by engine type



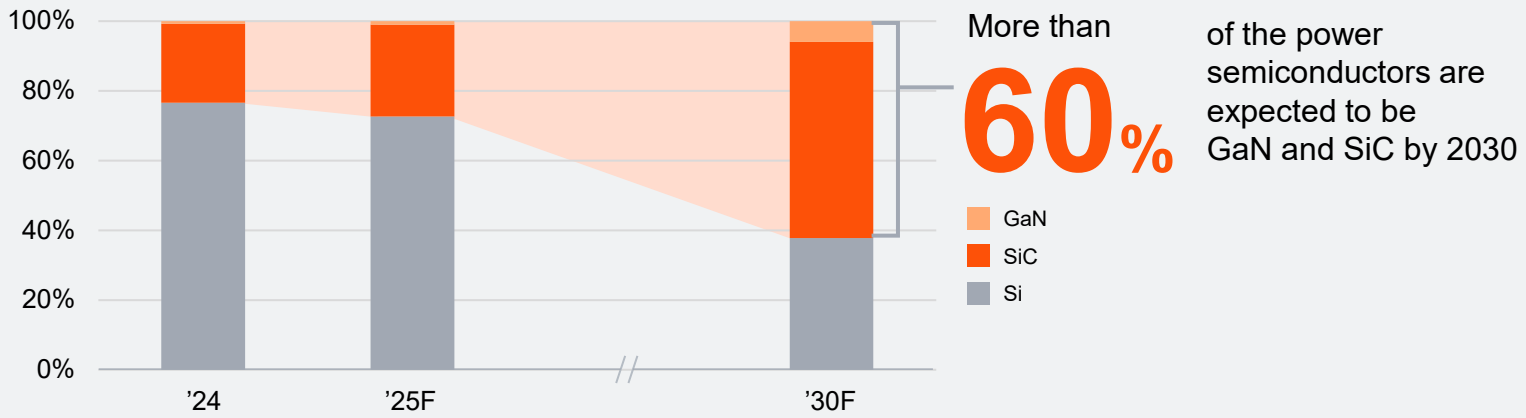
Source: PwC Autofacts, PwC analysis

More efficient? Stronger chips!

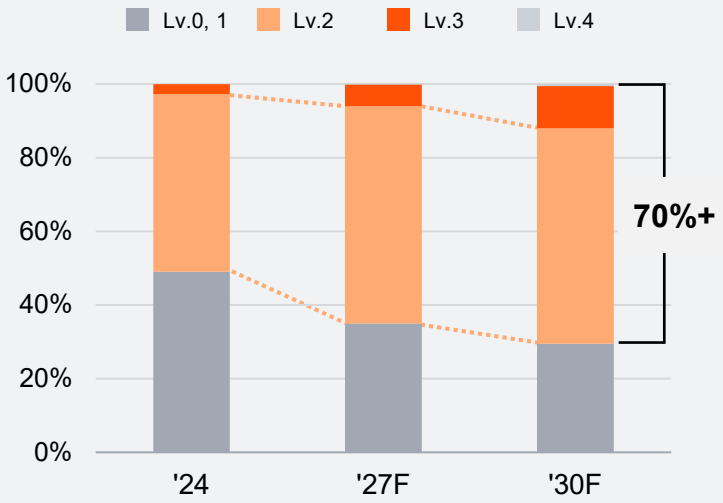
With the shift to electrification, efficient control of power becomes more challenging as engine drive and control, more functions such as autonomous driving and infotainment rely on electricity. Since driving an EV means repeated switching of high voltage power, demand for power semiconductors that can handle much higher power efficiently may surge. If chips can't withstand a high-voltage environment, significant operational failures such as fire can result.

This can lead to increased demand for new materials like silicon-carbide (SiC) and gallium-nitride (GaN). Compared to silicon chips, they can endure much higher voltages and offer faster switching speed, reducing power losses when switching. Automakers therefore deploy GaN for speed-critical, mid-voltage stages and SiC as the heavyweight workhorse for high-voltage, high-power paths—balancing efficiency, weight and total system cost across the EV powertrain.

Share of SiC and GaN power semiconductor in automotive

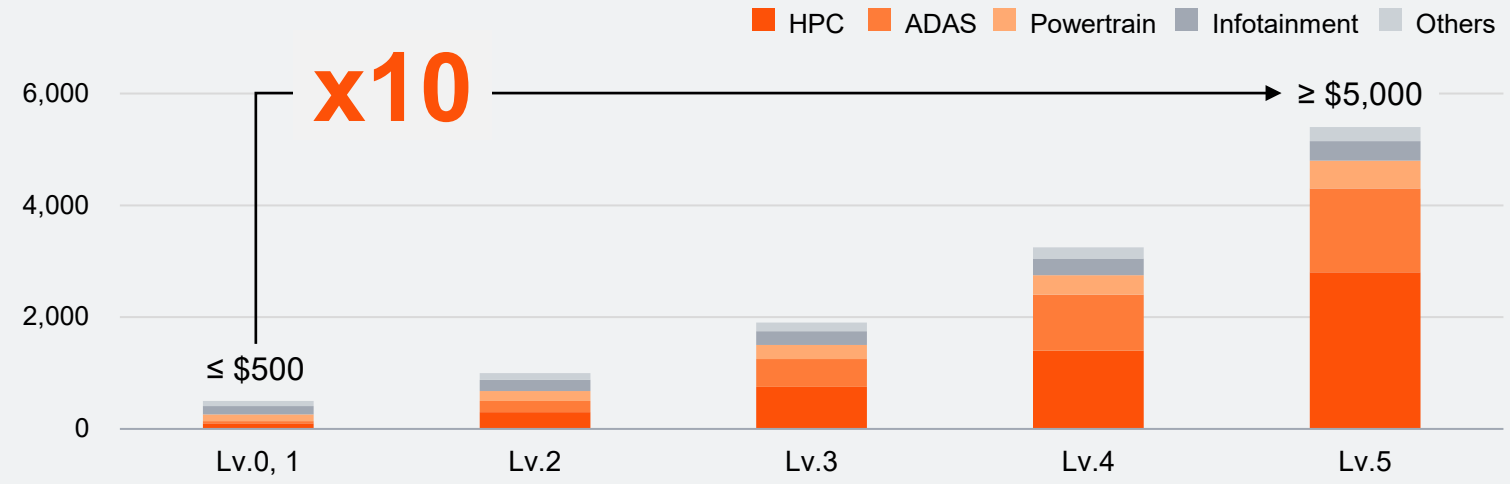


Level of driving automation



Source: PwC Autofacts, PwC Analysis

Semiconductor content by autonomous levels[1)] (Unit: $ per car)



1) Semiconductor content by autonomous levels was estimated using a bottom-up approach, aggregating component costs and market data by automation stage. These estimates may vary depending on future autonomous vehicle pricing trends and market conditions;

Self-driving technology is categorized into levels 0 to 5. level 0-1 offers driver assistance like collision and lane departure prevention. level 2 enables partial autonomy, such as maintaining distance from other cars in the road. From level 3, the vehicle can operate without constant driver monitoring. level 3 works on highways, level 4 extends to regular roads, and level 5 requires no driver at all, making a driver just like a 'passenger'. By 2030, most new cars may feature level 2, with level 3 likely exceeds 10% of total shipment.

The eyes, brains, and muscles of a car

As the level of autonomous driving advances, vehicles require a significantly greater capacity to gather and process data. This advancement increases complexity in the vehicle electronics architecture, driving up semiconductor costs for high-performance computing (HPC) and advanced driver-assistance systems (ADAS). In order to realize autonomous driving features, the automotives must be equipped with multiple sensors and connectivity chips to sense real-time information, computing chips to process that data, and electronic control units (ECUs) to take any action with the lowest latency.

Consequently, as vehicles become more autonomous, both the number of chips installed and the average price per chip rise significantly, fueling the growth of the automotive semiconductor market.

Software-defined vehicle changes how a car works

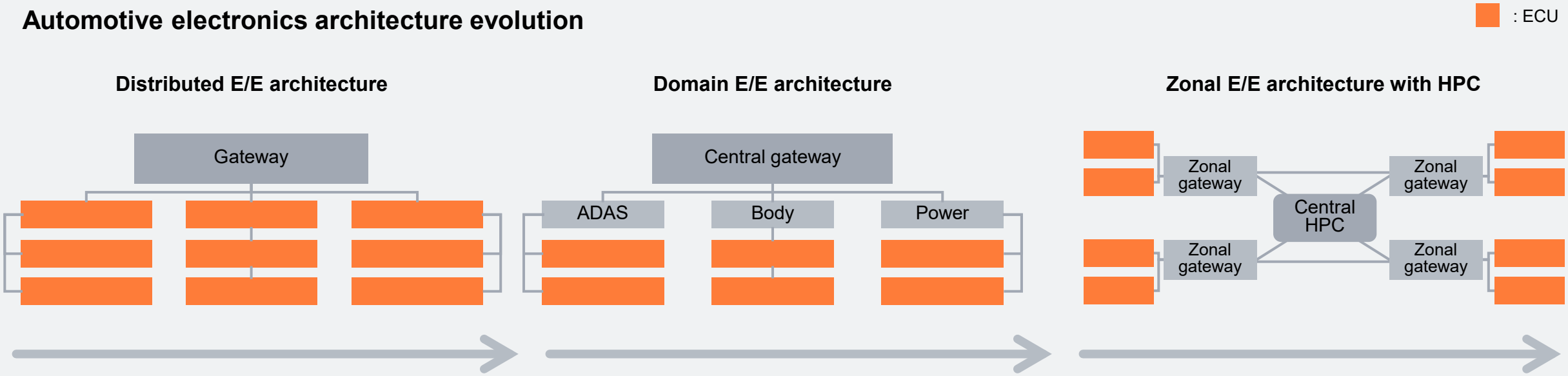
Have you ever woken up to new features on your smartphone after a software update? Now imagine the same concept with cars. Software-defined vehicle (SDV) enables new functions through updates without hardware changes.

With the rise of SDVs, the industry is moving toward a Zonal Architecture, where a central computer manages different zones of the vehicle. This approach further simplifies wiring, reduces physical complexity, and significantly enhances the stability of software updates.

This architectural transformation is reshaping the automotive semiconductor market as well. Electronic control units (ECUs), which previously handled individual functions, are now decreasing in quantity while taking on more complex roles. The focus is shifting from individual ECUs to high-performance SoCs, AI accelerators, and high-speed memory chips. Connectivity chips for real-time data transfer and security micro-controller units (MCUs) for software protection are also gaining importance.

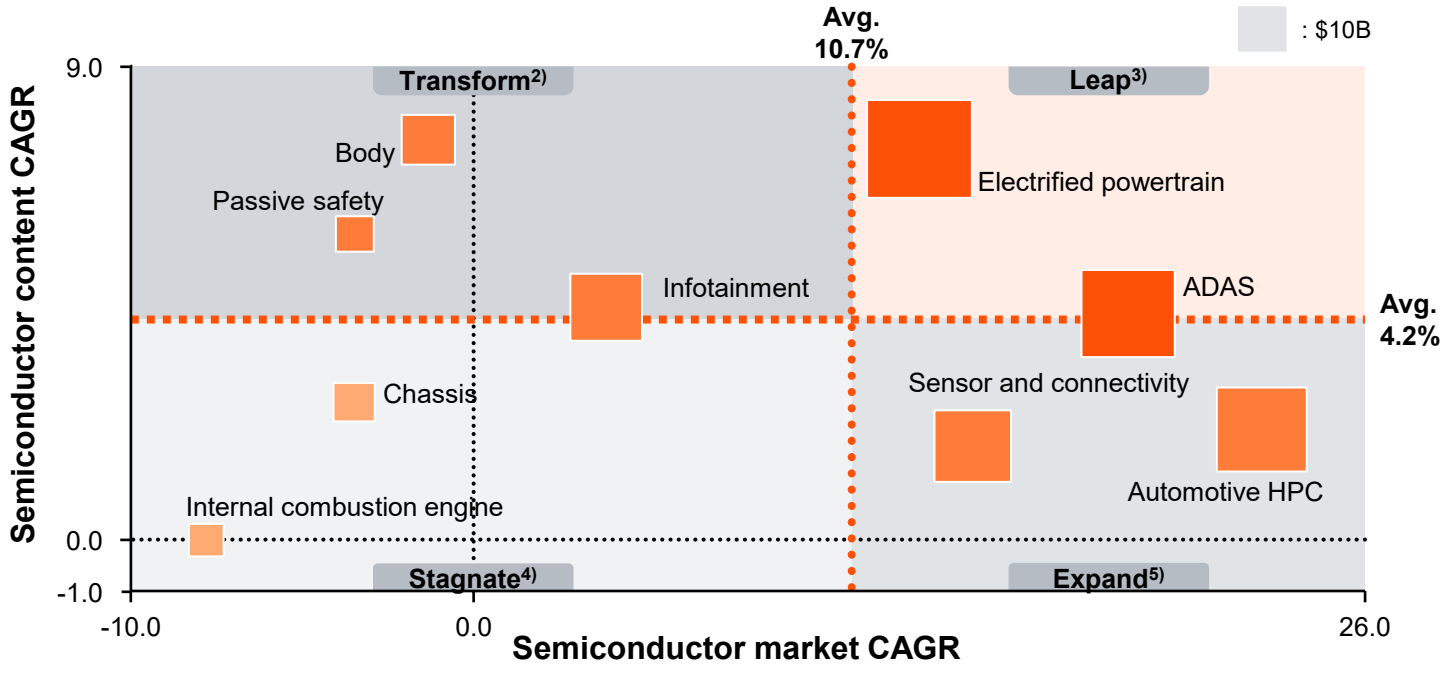
The automotive SoCs would integrate processing units such as graphics processing units (GPUs) and image-signal processors (ISP), but as the computing demands skyrocket and the architecture of cars move toward Zonal, the adoption of dedicated AI accelerators would increase as well.

Automotive electronics architecture evolution



Semiconductor demand by application, 2030[1)]

The bubble chart illustrates the projected semiconductor demand by major application for 2030. Dotted orange lines mark the average values on each axis, categorizing the applications into four quadrants.



1) The X-axis shows the compound annual growth rate (CAGR) of the semiconductor market in this end-market ('24-'30), the Y-axis indicates the compound annual growth rate in the proportion of semiconductors in the Cost of Goods Sold (COGS) ('24-'30), and the size of the squares represents the expected size of the semiconductor market ('30F).
2) As the technology and ecosystem are shifting towards semiconductors, the dependency on semiconductors within products is rapidly increasing.
3) The rapid growth of the semiconductor market and the quick expansion of the proportion of semiconductors relative to COGS can drive future semiconductor demand as a key area.
4) A market that has already entered the maturity stage, characterized by decline or slow growth, with a focus on stable operations rather than new investments or innovation.
5) The market itself is experiencing high growth due to mass production and sales, but the proportion of semiconductors relative to COGS is expanding more slowly by comparison.
Source: PwC analysis

Electrification and autonomous

These two trends have a significant impact on increasing the demand for semiconductors. In the case of electrified powertrains, there is a major influence on power semiconductors (such as insulated-gate bipolar transistors(IGBTs) and SiC chips), while autonomous driving predominantly affects ADAS ECUs. Moreover, the demand for electric vehicles and autonomous vehicles is increasing simultaneously.

Additionally, as autonomous driving technology and SDV trends advance and expand, the demand for related semiconductors such as automotive HPC, sensors, and connectivity chips is expected to grow. Moreover, there are expectations for upgrades in semiconductors related to body, infotainment, and passenger safety to improve the in-car environment.

In the case of chassis and internal combustion engines, however, the market size is expected to gradually decline due to reduced technological innovation and a stagnating market size.

Semiconductor demand intensity for applications by 2030

Applications			Demand intensity	Demand trends
Driving assistance	ADAS	L		Increasing complexity of environmental perception, signal processing, and AI/deep learning in autonomous driving is leading to higher demand for high-performance processors.
	Sensors and connectivity	E		Higher-level autonomous cars can require more cameras, radar, LiDAR, and other sensors to provide redundancy and cross-validation.
Digital cockpit	Infotainment	T		The integration of digital cockpits, the growing adoption of multiple displays, and the expansion of features require the demand for increased processing power.
	Automotive HPC	E		Domain integration and zone architectures are increasing demand for high-performance computing systems instead of distributed ECUs.
Body · Chassis	Body	T		Adaptive front-lighting, zonal climate modules, smart glass and haptic seats expand the need for networked sensors, brushless DC (BLDC) drivers and mixed-signal MCUs.
	Chassis	S		Centralized chassis controllers integrate ABS, ESC, e-axle torque vectoring and steer-by-wire, sharing wheel-speed and inertial sensors while cutting standalone ECUs.
Powertrain	Electrified powertrain	L		EVs require more complex power chips, which are key components for electric motors and inverters as well as for sophisticated battery management system (BMS) control ICs.
	Internal combustion engine	S		Demand for engine MCUs and exhaust-gas sensors is expected to remain flat or decline gradually as OEM fleets electrify.
Others	Passive safety	T		Stricter regulations can drive incremental growth in radar, vision processors and MEMS crash sensors (airbag accelerometers, pressure sensors).

L Leap E Expand T Transform S Stagnate

Weak Strong

Server and Network

Since the surge of generative AI (Gen AI) applications in 2022, the amount of data generated and processed has expanded at an exponential rate. From AI-driven automation and IoT proliferation to the increasing intelligence of vehicles and industrial systems, data is no longer just an asset—it is the foundation upon which modern digital infrastructure is built.

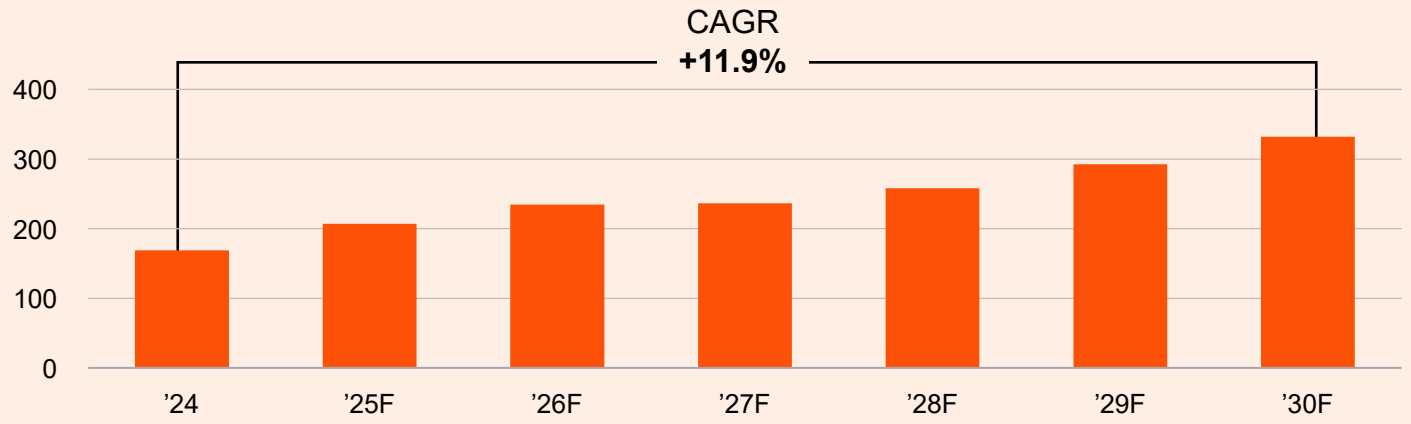
By 2030, the increasing demand for computational power is expected to further accelerate the growth of CPUs, GPUs, and AI accelerators, with HBM continuing to be a crucial component in supporting them. Especially for servers, major tech companies including cloud service providers already started to develop their application-specific integrated circuits (ASICs) to reduce operational costs. At the same time, the expansion of 5G may drive the need of computing powers for network equipment and GaN based radio-frequency (RF) chips to enable ultra-fast, low-latency communication.

Server and network can be the backbone of the intelligence permeating applications around us, powered by the continuous advancements of semiconductors.

AI Data Centers and Next-Gen Connectivity

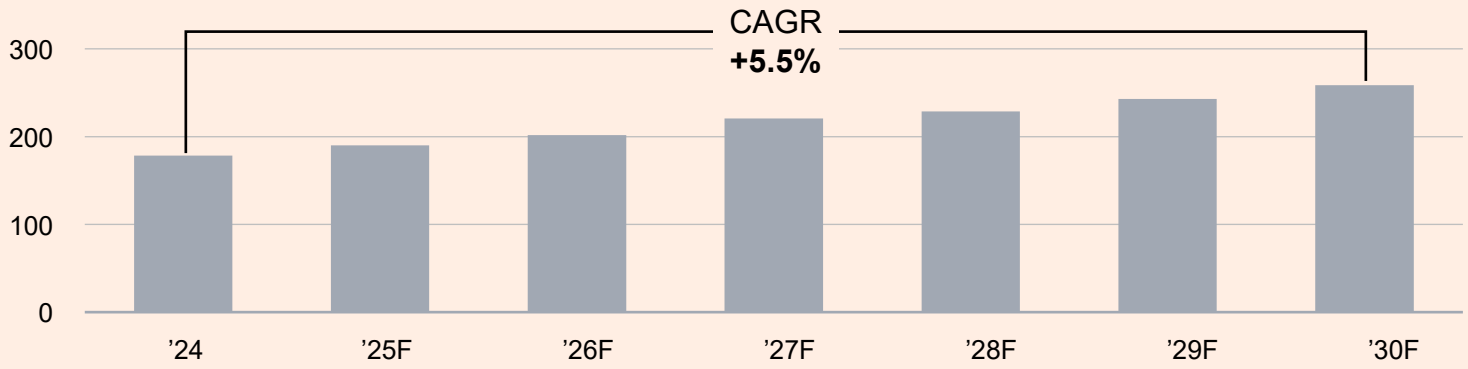
The rapid growth of AI, connectivity, and customer adoption of advancing technology has led to increased demand for data centers and the servers within them to process the data. With the investment of cloud service providers, collocation centers, and telecommunication companies for data centers, the global server market is expected to reach over $300B in 2030.

Global server market (Unit: $ Billion)



Source: Gartner, Statista, PwC analysis

Global networking infrastructure market (Unit: $ Billion)



Source: Gartner, Statista, PwC analysis

At the same time, the demand for infrastructure supporting inter-server and -node connections is rising.

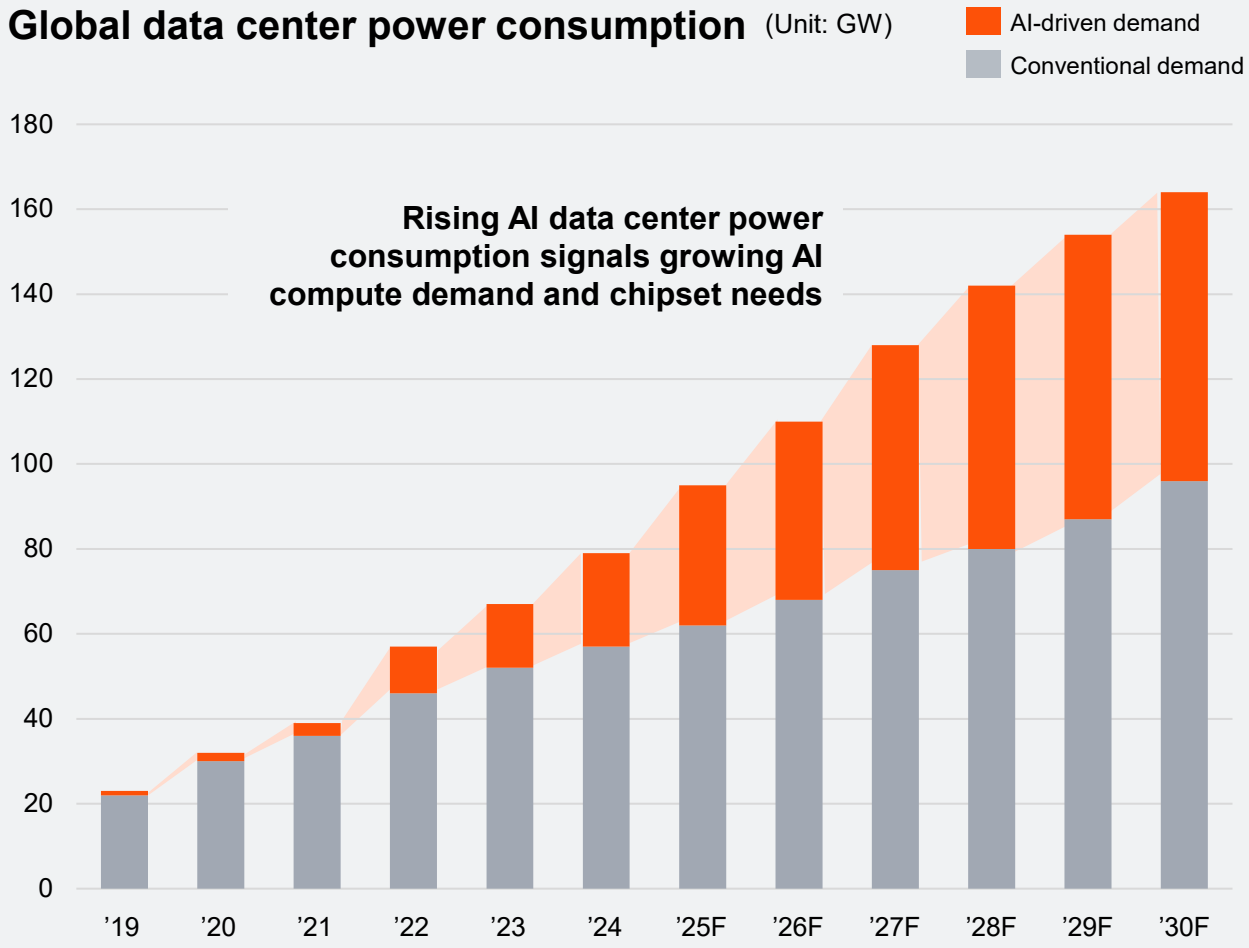
The need for faster, more extensive, and reliable connectivity fuels the market growth for devices such as routers and modems, included as a backbone and infrastructure. This trend extends beyond a single application, encompassing enterprise, public, and private networks.

Faster, bigger, smarter data centers

It is cliché, but true, that we are living in the world of data and connectivity now. More and more devices are interconnected than ever before, including cars, home appliances, smartphones, and PCs. In addition to the growth of number of devices connected, consumers are demanding higher-quality entertainment such as AR/VR/XR gaming and seamless video streaming. Moreover, the introduction of 'ChatGPT' in November 2022 became a motivator for both companies and individuals to actively utilize AI services in various applications they can possibly imagine.

These applications generate and require astronomical amount of data, and we've witnessed just the start of it. With high demand for gaming and video streaming, and most importantly, with the rising demand of AI, global data centers are expected to more than double their power consumption by 2030.

Data centers are a crucial resource for storing, processing, and managing data. They used to focus on providing services for enterprises, but with rising demand, they have achieved hyperscale status, providing internet as a service. Now with the demand of AI-specific applications, Data centers are once again evolving into AI-data centers, enhancing managers' ability to provide lossless services to data center users.



Source: IEA, PwC analysis

The future of intelligent infrastructure

As AI applications push the required data volume for processing, and as the scale of data centers grows in response, operational expenses for cooling and electricity have reached astronomical levels. Companies are now seeking ways to operate more cost-effectively.

The first way to do so while boosting AI performance is to utilize data-center-specific chips. These chips are crucial for achieving high performance because they are built to handle the intensive computational demands of data processing more efficiently than general-purpose processors. To get the desired level of performance, companies are turning to these specialized chips to meet their needs.

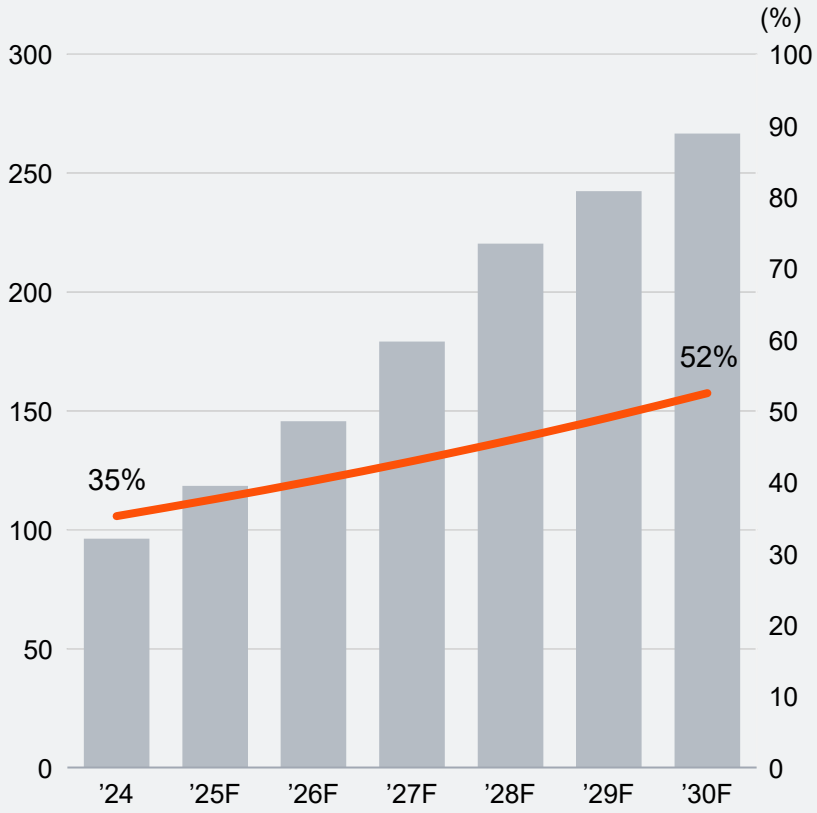
However, even if designed specifically for data centers, standard chips are designed for multiple customers and thus contain functions that a given customer might not use. Therefore, big techs like cloud service providers are developing their own AI accelerators specifically designed for their own data center applications.

By developing AI chips tailored to specific workload, companies can reduce cost and power while achieving higher performance. The demand for AI accelerators is expected to rise as the need for cost reduction grows with increased data-processing demand.

Therefore, the revenue share of AI accelerators among chips used in data centers can grow at a very fast pace, reaching around 50% of total data center chips.

In addition to AI accelerators, other data-center-specific chips such as data processing units (DPUs) and advanced memory chips such as HBM can also rise. HBM reduces a data processing bottleneck, supporting high-performance GPUs, and data processing units (DPUs) offload CPU networking workloads by handling data transmission. Sales of these data-center-specific chips may continue to grow as they become essential.

AI accelerators in the data center (Unit: $ Billion)



Source: PwC analysis

Next generation Wi-fi and mobile network

When data traffic increases, it's not just data centers that need upgrades. Standardized network protocols for connecting devices and delivering data may need enhancement as well.

Your device might be connected via Wi-fi or cellular data right now. The 'G' in 4G/5G stands for 'Generation', upgraded roughly every decade from 2G in the 1990s for voice and short message service (SMS) to 3G for media in 2000s, and to the high-speed 4G (2010s) and 5G (2020s). Similarly, the Wi-fi standard has evolved.

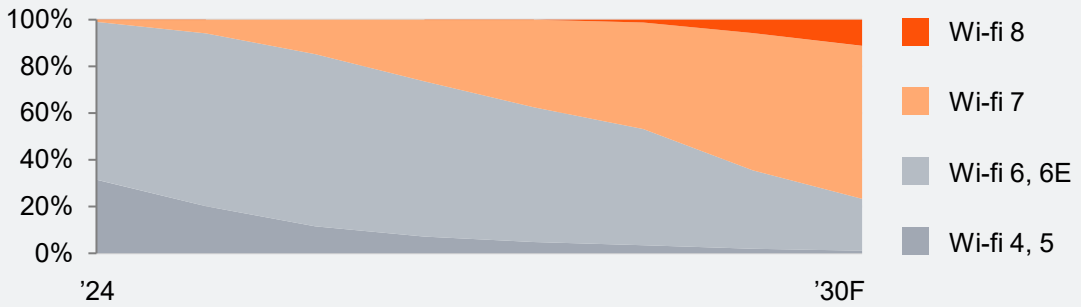
When the variety and volume of wireless data expands, it can require broader bandwidth (larger traffic lanes) and new frequency bands (new routes). It's just like expanding roads or constructing new highways as traffic volume grows. Current Wi-fi and 4G speeds may seem enough, but the surge in data may eventually push us toward higher standards.

With the expansion of 5G and future 6G networks, speed could be up to 20 to 100 times faster than 4G. Technology like non-terrestrial networks (NTN), which use satellites as base stations, may further enhance network coverage.

Likewise, transitioning from Wi-fi 6/6E to 7 can enable faster data through wider channels. Especially with multi-link operation (MLO) technology, Wi-fi 7 can enable simultaneous use of multiple routes, enabling a fast and stable connection even if a certain route were to experience interference – ideal for gaming and video streaming.

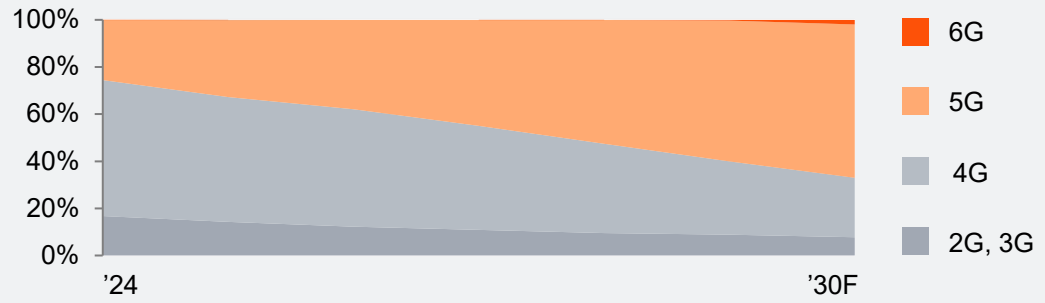
As connectivity standards advance, network devices and infrastructure are also updated. Although these changes are not as visible as server upgrades, there will be a continuous demand for improved network equipment and infrastructure in the future.

Generation of Wi-fi by portion of connected device



Source: Wi-fi Alliance, PwC analysis

Cellular standards by portion of connected mobile device



Source: ITU, PwC analysis

Powering data connectivity

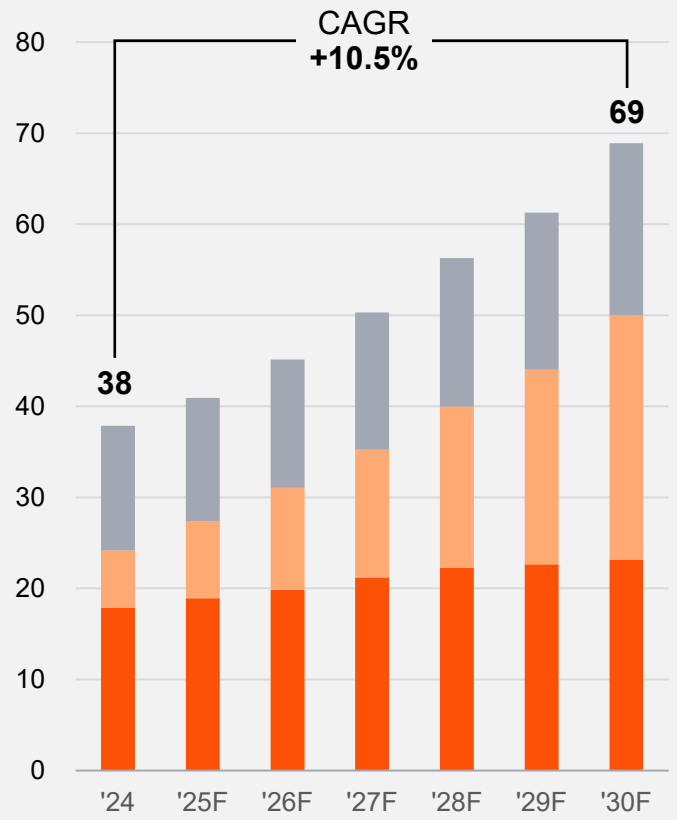
Semiconductor performance must advance in step with upgrades in connectivity standards. Semiconductors are critical to preventing issues such as poor connectivity in elevators or inconsistent signal strength depending on location. Semiconductors can amplify signals so that they have better reach with no distortions.

Although semiconductors remain essential, the market for semiconductor components supporting 5G is expected to grow at a relatively slower pace compared to that for data centers. The 5G infrastructure in many countries has largely matured, leading telco companies to prioritize investments in data centers. As a result, growth in semiconductors for telecommunication equipment is likely to remain moderate until 2030.

On the other hand, with increasing data traffic and the widespread adoption of AI in enterprises, there has been a notable rise in demand for switches, routers, and smart network interface cards (NICs) to support cloud-service operations in data centers. This shift is fostering growth in data center networking equipment, the local area network (LAN) and wide area network (WAN) markets. Consequently, semiconductors catering to these areas are projected to see robust growth through 2030.

The growing volume of data can require more advanced and sophisticated networking equipment. As a result, the demand for ASICs and field programmable gate arrays (FPGAs) is increasing, and more telecom equipment companies are likely to develop their own chips.

Networking-equipment semiconductor market (Unit: $ Billion)



CAGR, 2024-30F

Telecom	+5.5%
Data center	+27.4%
Enterprise	+4.4%

Source: PwC analysis

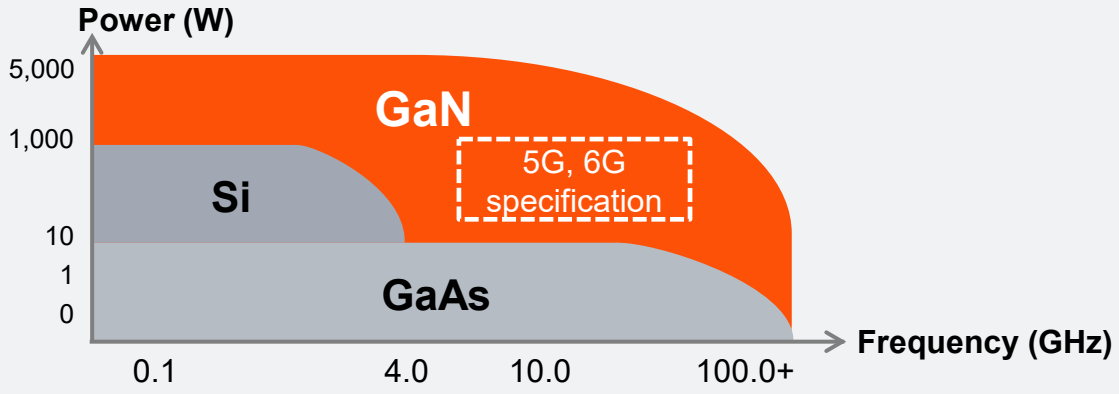
The shift to GaN RF chip in telecom market

RF chips perform the critical function of amplifying wireless signals for transmission. The advent of millimeter-wave 5G requires semiconductors that are capable of handling high frequency ranges, which GaN and gallium arsenide (GaAs) offer. Moreover, unlike GaAs, GaN can handle high power and high frequencies at the same time, making it well-suited for the demanding specifications required by base stations. The strengths of GaN semiconductors are anticipated to shine in sectors that require reliable communication, such as base stations, defense, and aerospace.

As of 2025, while the growth of 5G telecom equipment may slow down as these technologies mature in developed countries, there remains significant global growth potential, with continued demand for upgrading existing base stations. Even though GaN RF chips are more expensive than silicon options, the market for GaN RF chips is poised to continue growing. GaN already accounts for over half of the RF chips in telecom equipment market and is expected to capture up to 90% of the market in the future. However, this doesn't imply that silicon RF chips can be entirely replaced. Base stations usually amplify signals through several stages, making silicon-based chips a cost-effective choice for lower frequency applications.

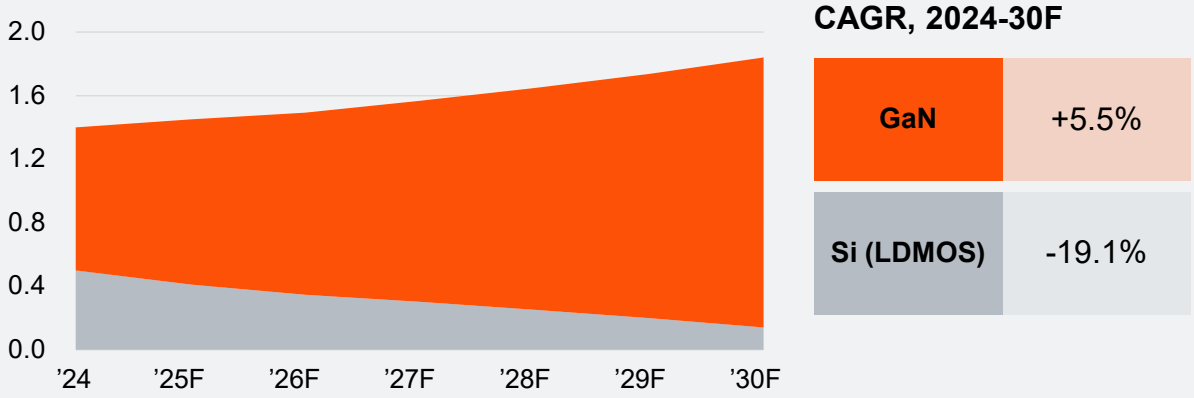
Optimal frequency and power by RF material

(Per Total Base Station Antenna)



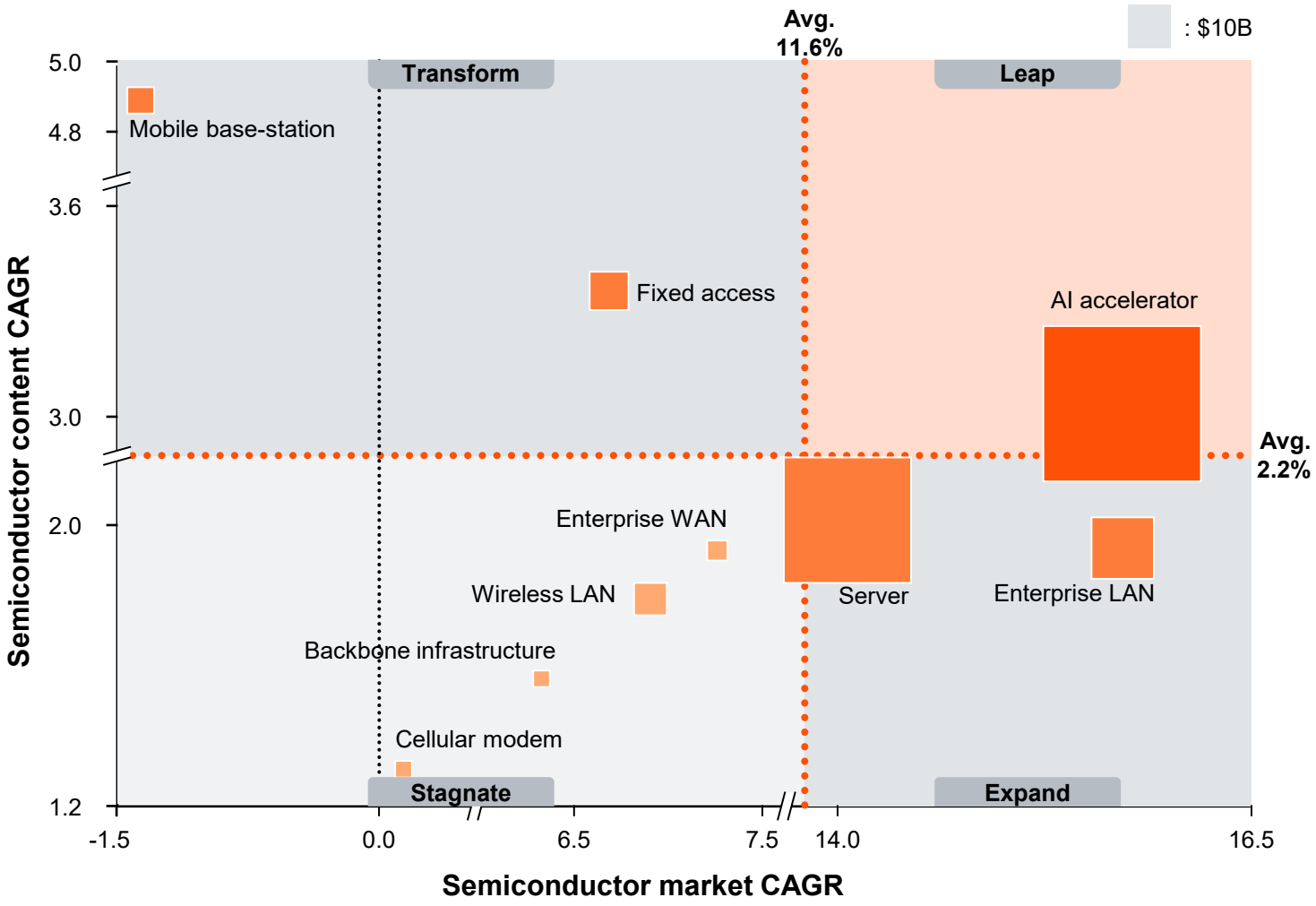
Source: IEEE, PwC analysis

RF semiconductor market in telecommunication (Unit : $ Billion)



Source: PwC analysis

Semiconductor demand by application, 2030



AI and connectivity

AI models are becoming more complex, and datasets are expanding, leading to a rising need for high-speed data transfer both within data centers and across networks. As a result, there is a significant increase in demand for servers that can manage this growing data traffic, fueling market growth.

The demand for accelerator cards, including AI accelerators, is surging due to the increased need for advanced servers, improved AI capabilities, and custom designs. Additionally, enterprise LAN demand is set to grow to handle faster data traffic. With evolving communication standards, the share of chips in the total cost of mobile base-station and fixed access equipment is expected to increase.

Meanwhile, enterprise WAN, wireless-LAN (WLAN), and backbone infrastructure are steadily expanding in market size due to heightened data traffic and communication needs. Despite this growth, the proportion of semiconductor costs is unlikely to increase significantly, as major investments in telecommunications infrastructure have already been made.

Semiconductor demand intensity for applications by 2030

Applications			Demand intensity	Demand trends
Server		Server (E)		The growth of the server market due to AI workloads is leading to higher demand for high-performance CPUs and memory within data centers.
		AI accelerator (L)		The demand for specialized GPUs, FPGAs, and ASICs is rapidly increasing due to the growth of artificial intelligence and machine learning.
Network	**Wired**	Fixed access (T)		Specification upgrades in system chips related to security and encryption, along with the expansion of switching capabilities, are increasing the semiconductor content per unit
		Enterprise LAN (E)		Digital transformation and IoT expansion are driving demand for components such as physical layers (PHYs) and switch SoCs.
		Enterprise WAN (S)		The WAN market is more mature and focused on high-speed, wide-area connectivity compared to the LAN market, resulting in longer investment cycles and slower market growth,
		Backbone infrastructure (S)		Since the infrastructure is already extensively deployed both nationally and globally, relatively small-scale upgrades are generally needed, leading to limited growth in chip demand.
	Wire-less	Wireless LAN (S)		While a shift to Wi-fi 7 is anticipated by 2030, the relatively minor functional changes suggest that the growth in demand for related chips will likely be modest.
		Cellular modem (S)		Generational upgrade cycles, aimed at enabling a stable communication environment, tend to be relatively long, with no major changes expected until 2030.
		Mobile base-station (T)		Large-scale infrastructure investment has peaked for 5G, but the introduction of high-performance chips driven by 5G-Advanced upgrades is likely to gradually increase demand.

Weak Strong

L Leap E Expand T Transform S Stagnate

Home Appliances

Although the home appliances market is relatively saturated, AI and IoT technology are making appliances smarter and providing new consumer experiences. Moreover, new appliances are gaining market traction, such as augmented reality(AR) / virtual reality(VR) and wearable devices.

The growth of AI appliances may significantly increase the demand for AI processors and semiconductors such as power management ICs (PMICs), enabling both power efficiency and personalized experience. Wearable devices for gaming and healthcare can simultaneously drive the semiconductor market for sensors, connectivity ICs, processing units, and more. Lastly, the expansion of IoT will likely fuel the demand for connectivity ICs capable of supporting diverse communication protocols between the electronics.

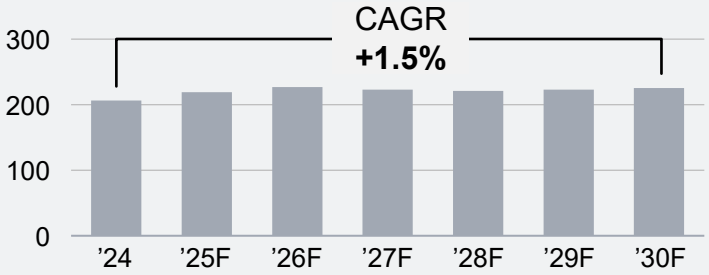
Semiconductors can serve as the foundation for the ongoing evolution of appliances, fundamentally transforming the 'smart experience' available in our homes.

Traditional home appliances vs. new entrants

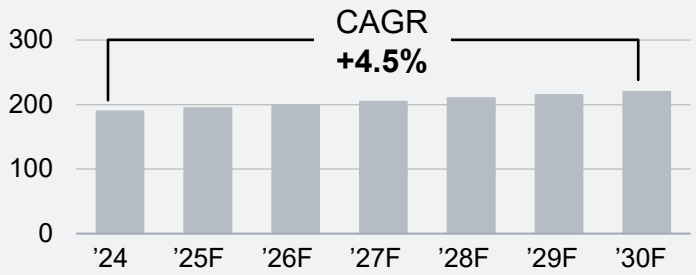
While the home appliance market is relatively mature, the integration of IoT and AI technologies into traditional appliances—such as refrigerators—can accelerate consumers' replacement cycles. Simultaneously, innovative products such as AR/VR headsets and personal robots are beginning to penetrate the appliance market.

Traditional appliances market (Unit : Million)

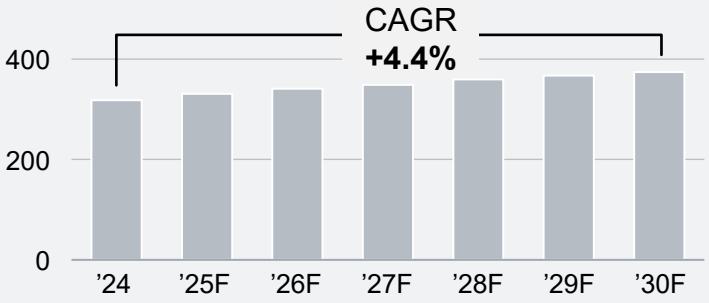
TVs



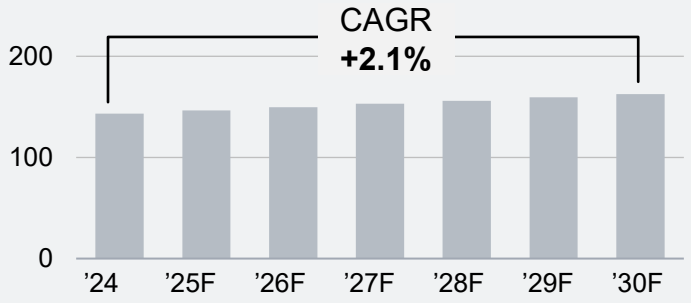
Refrigerators



Air conditioners



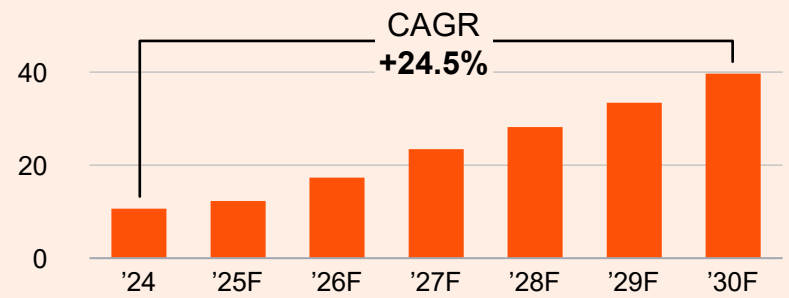
Washing machines



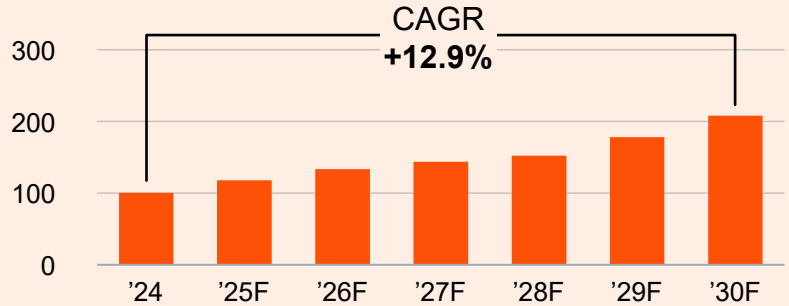
Source: Gartner, Statista, PwC analysis

New appliances market (Unit: Million)

AR/VR



Personal robots



Smart, strong, and energy-efficient: The next wave of home appliances

AI-powered home appliances

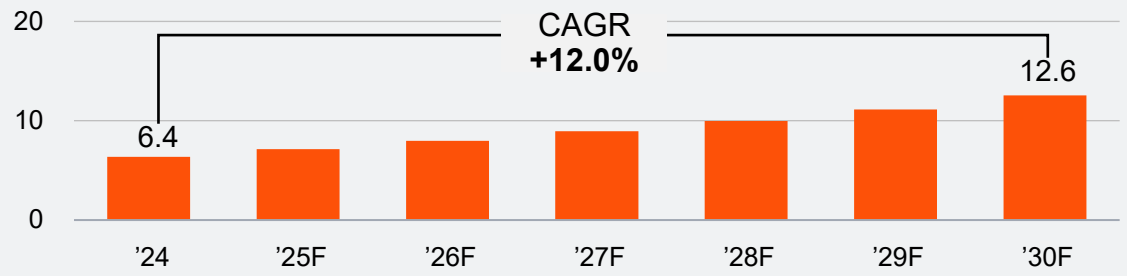
	Computing Power	Power Efficiency	Smart Features
TV	↑	↑	▪ Upscaling and automatic improvement of video (4K → 8K) / audio quality
Refrigerator	↑	↑	▪ Tracking food expiry dates ▪ Sensors improve power efficiency real-time
Personal robot	↑	→	▪ Robot cleaners with automatic route and cleaning mode ▪ Pet robots with AI assistance
AR/VR	↑	→	▪ Upscaling of video/audio quality with low-latency ▪ Building of smart-home hub
Air conditioner	→	↑	▪ AI climate control with real-time weather and room sensor
Washing machine	→	↑	▪ AI-based fabric detection for automatic wash cycle setting

The rise of smart experiences in smartphones, PCs, and cars has raised consumers' expectations at home as well—and not only in recently emerged appliances such as AR/VR devices. Although shipments of traditional appliances have not grown exponentially, AI features are integrated into TVs, robot vacuums, and refrigerators, fostering the demand of AI processors in the home-appliances market.

In addition to performance, power efficiency is critical. AI can also improve the energy-efficiency of appliances. This is especially important as power efficiency standards for appliances are getting tougher, including regulations on power during standby mode. This growing focus on efficiency is expected to drive increased demand for application processors designed for AI workloads, as well as for PMICs and compact battery management ICs that optimize device power usage.

SoCs in AI home appliance

(Unit: $ Billion)



Source: PwC analysis

The rise of a hyperconnected home experience

Home appliances are now connected to each other more than ever before, setting a new standard for smart experiences. Devices like washing machines, refrigerators, lights, AI speakers, and robot vacuums now communicate with each other to create a seamless smart-home experience. This trend is further accelerated by the introduction of the Matter smart-home standard in 2022, which enables devices from different manufacturers to communicate seamlessly.

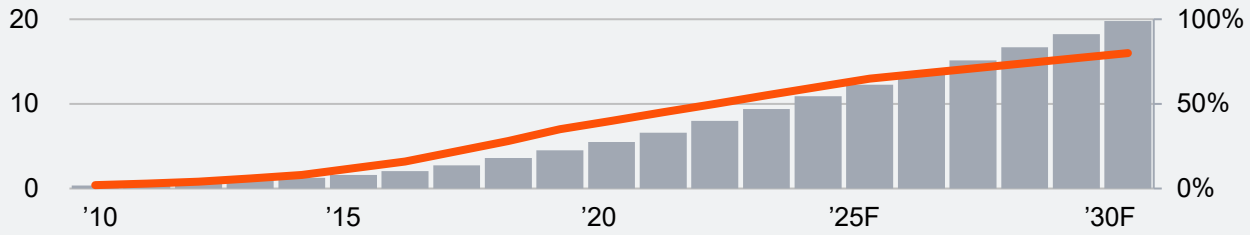
As IoT connectivity becomes ubiquitous in appliances, more devices will be equipped with connectivity ICs. Furthermore, these chips—whether standalone SoCs or integrated within application processors (APs)—are evolving to support multiple communication protocols.

For a smooth communication experience, devices use multiple channels depending on the situation. Matter supports Bluetooth, Wi-fi, and a protocol called Thread for direct device-to-device communication. For example, Wi-fi is ideal for large, high-speed data transfers, making it perfect for smart TVs and smart refrigerators with displays. Bluetooth is used for short-range communication, while Thread, which features energy efficiency, can be suitable for battery-powered devices or smart speakers that need to connect directly to other appliances.

In conclusion, as appliances increasingly adopt and expand their smart IoT capabilities, the demand for connectivity ICs is expected to rise.

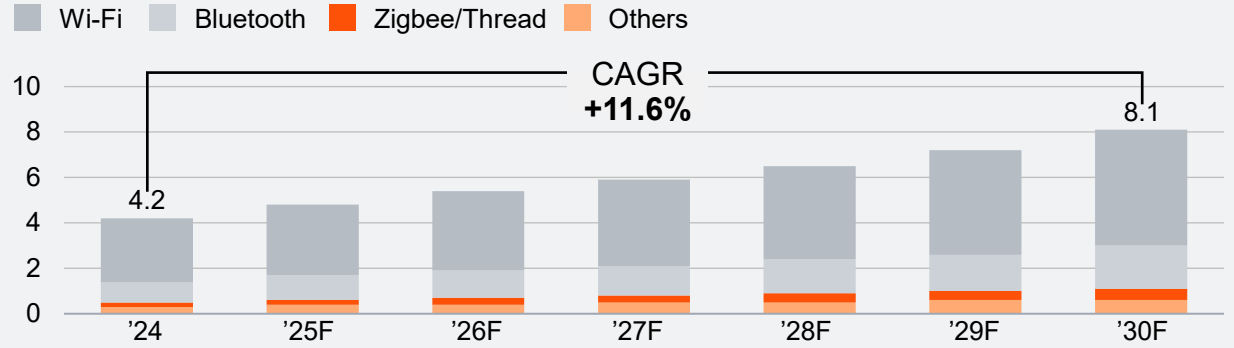
Number of connected home appliance

(Unit: Total home appliances in billion, share of connected home appliance)



Source: Statista, PwC analysis

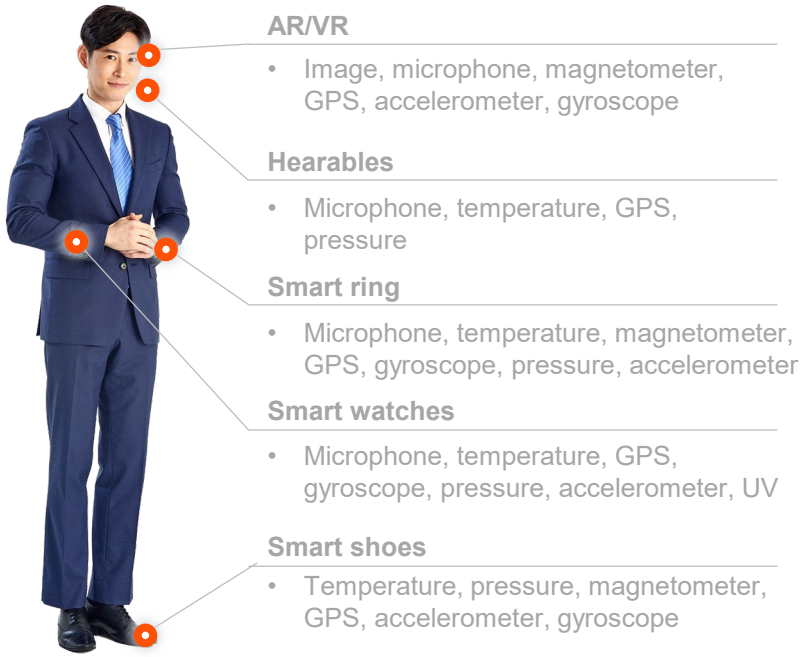
Connectivity ICs in home appliance (Unit: $ Billion)



Source: PwC analysis

Connecting the boundaries of the real and virtual

Examples of sensors in wearables



AR/VR
- Image, microphone, magnetometer, GPS, accelerometer, gyroscope

Hearables
- Microphone, temperature, GPS, pressure

Smart ring
- Microphone, temperature, magnetometer, GPS, gyroscope, pressure, accelerometer

Smart watches
- Microphone, temperature, GPS, gyroscope, pressure, accelerometer, UV

Smart shoes
- Temperature, pressure, magnetometer, GPS, accelerometer, gyroscope

How many devices are you wearing right now? Wearables—from earphones and headphones to smartwatches, fitness bands, AR/VR devices, and healthcare gadgets—have become an integral part of our lives. As a result, the demand for sensors is rapidly increasing,

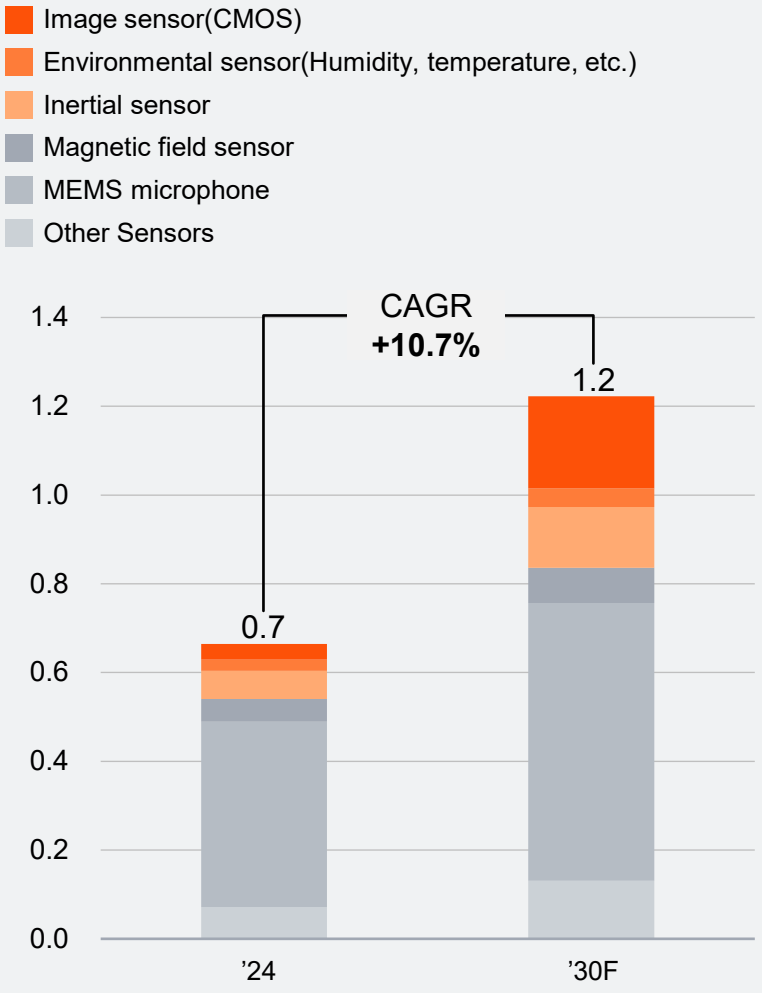
and AR/VR devices may utilize various sensors to track eyes and motion for user interaction along with cameras and microphones for an augmented-reality experience. Wearable healthcare devices also use multiple sensors to monitor health, movement, and the environment. Inertial sensors track the speed of your movement, with magnetic field sensors supporting the analysis by sensing the motion of your body. New sensors such as non-invasive blood glucose sensors using saliva or photoacoustic methods may continue to emerge.

Data collected from these sensors can often be noisy and irregular. Biological signals fluctuate with movement, and external interference from noise and electromagnetic fields can disrupt accuracy.

To address these challenges, the semiconductor industry is focusing on developing advanced processors and wearable-specific SoCs as well, enabling more efficient sensor data processing and improving overall device performance.

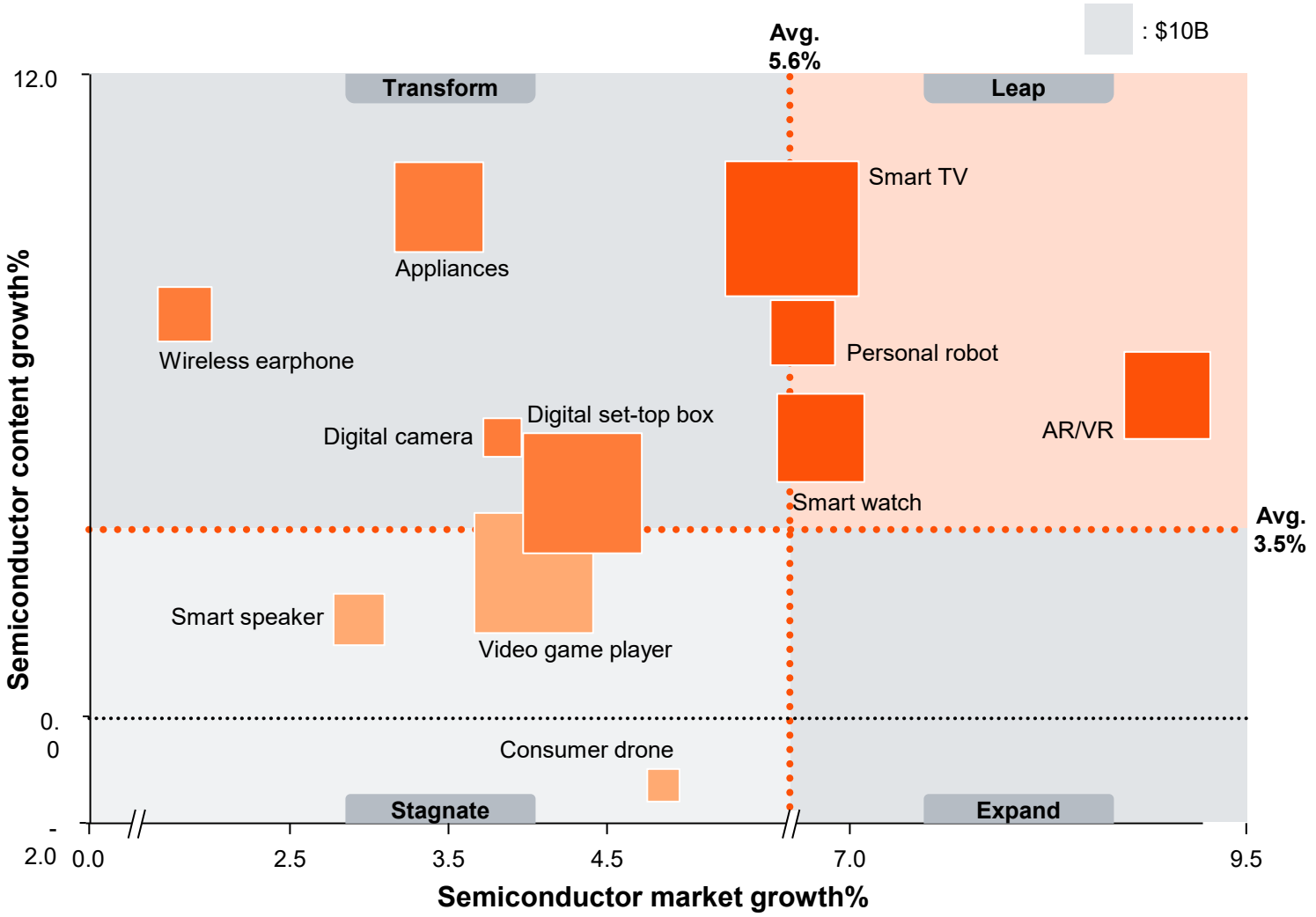
Sensor ICs in wearable devices

(Unit: $ Billion)



Source: PwC analysis

Semiconductor demand by application, 2030



Smartification and IoT

Home appliances are becoming increasingly smart and connected. Televisions —the largest-volume category—now feature AI-driven picture and sound enhancement, smart home control, and personalized content recommendations, all of which are pushing up demand for advanced semiconductors.

Major appliances and digital set-top boxes are also increasing the share of semiconductors due to an increase in smart features and connectivity options, while wireless earphones and digital cameras are using more semiconductors due to functional expansion and sophistication.

On the other hand, smart speakers and consumer drones face lower innovation pressure, and because much of their cost lies in non-semiconductor components, their incremental semiconductor demand remains relatively modest.

Semiconductor demand intensity for applications by 2030

Applications		Demand intensity	Demand trends
TV	Smart TV L		The rapid spread of AI TVs is boosting chip demand, especially for TV SoCs and display driver ICs, driven by expanded features, high-resolution and high-refresh displays.
Wearables	AR/VR L		Demand is increasing for high-performance processors for 3D rendering, data processing, and complex visual effects, along with real-time environmental sensors.
	Smart watch L		As smart watches evolve into healthcare devices, demand for advanced sensor chips (such as heart-rate monitors, inertial measurement units, and GPS) is steadily growing.
	Wireless earphone L		Wireless earphones are evolving into smart wearables, driving increased adoption of low-power digital signal processors(DSPs) and lightweight NPUs for voice processing and AI features.
Video game player S			The video game console volume has become saturated, with growing emphasis on software, subscriptions, and cloud gaming, limiting further growth in semiconductor demand.
Others	Digital camera T		Unit shipments keep declining, yet premium models drive demand for stacked CMOS image sensors and high-end image signal processors(ISPs), keeping revenue roughly stable.
	Smart speaker S		Core volumes have plateaued, but on-device large language models are adding NPUs and higher performance DRAM, modestly reviving chip content per unit.
	Digital set-top box T		Legacy pay-TV set-top boxes are declining; growth shifts to high-integration over-the-top (OTT) streaming SoCs with Wi-fi 6/6E.
	Appliances T		The widespread adoption of connected appliances, along with improved energy management efficiency, is driving the demand for connectivity ICs and PMICs.
	Consumer drone S		Unlike industrial drones, which are function-focused, the emphasis for consumer drones is on cost and battery efficiency, limiting their potential for demand growth.
	Personal robot L		The growing adoption of household robots, such as cleaning and educational robots, along with their enhanced functionalities, is driving the demand for ASIC and connectivity ICs.

Weak Strong

L Leap E Expand T Transform S Stagnate

Computing Devices

While the smartphone and PC markets have matured, their value proposition is shifting toward high-performance models that redefine user experience. The emergence of AI-driven applications—ranging from advanced photography and gaming to real-time AI assistants—is set to reignite market growth, giving rise to a new generation of AI PCs and AI smartphones

With the increasing demand for AI-integrated computing devices, the adoption of neural processing units (NPUs) is expected to accelerate, complementing the advancements in GPUs, CPUs, and image signal processors (ISPs) within application processors. Meanwhile, Low-power double data rate (LPDDR) memory technology may continue to evolve, enhancing performance, miniaturization, and power efficiency for next-generation PCs and smartphones.

With AI applications becoming widespread, coupled with growing demands for higher-resolution displays, powerful computing capabilities, and increased storage, PCs and smartphones will likely continue to drive semiconductor industry growth.

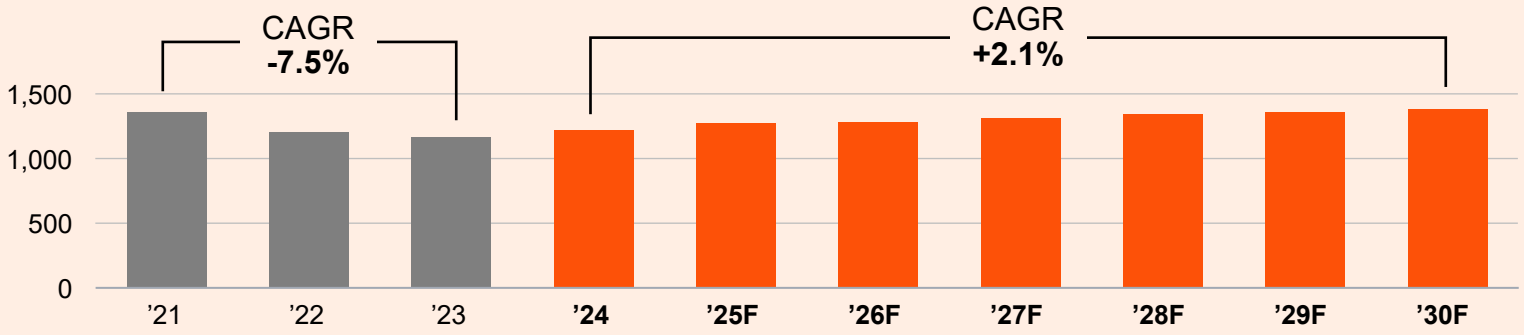
Computing devices' regrowth through evolution with AI

The smartphone and PC markets have been relatively saturated compared to other applications such as automotive and data centers.

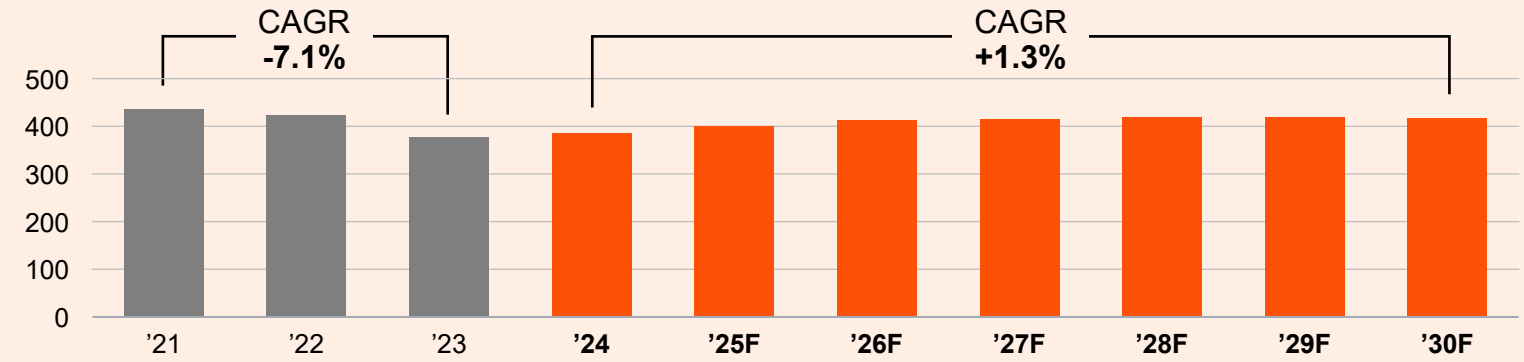
However, as AI pervades in our daily lives, there has been a trend to operate AI services directly on personal devices. This shift has driven a growing demand for AI-powered PCs and smartphones as users seek devices capable of handling advanced AI applications seamlessly.

The increasing integration of AI features, from virtual assistants to on-device machine-learning tasks, is revitalizing the market, creating new growth opportunities for device manufacturers and semiconductor companies.

Global smartphone market (Unit: Million)



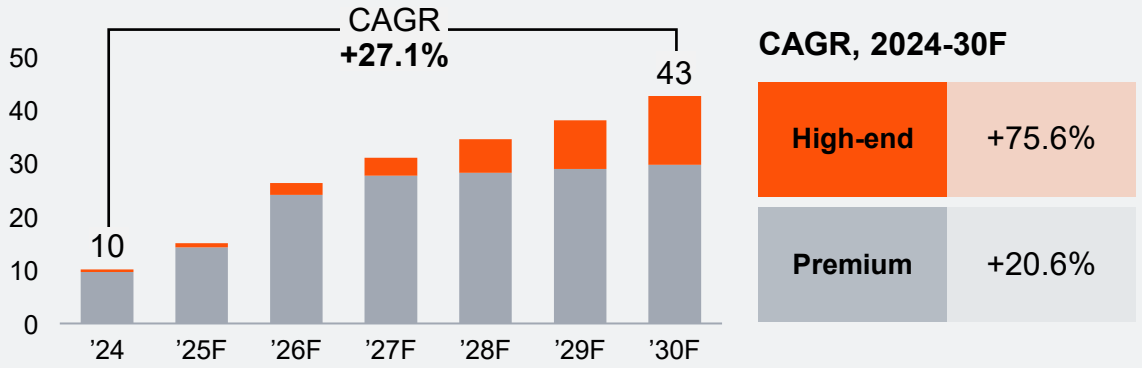
Global PC and tablet market[1)] (Unit: Million)



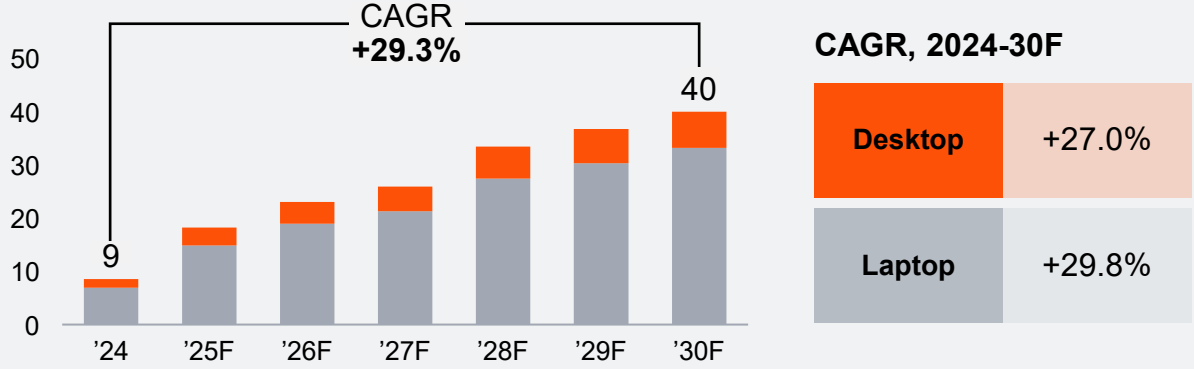
1) PC and tablet market refers to the total sales of desktops, laptops, and tablets combined
Source: Gartner, Statista, PwC analysis

On-device AI unlocks the next potential of smartphones and PCs

AI-capable chips in smartphone[1)] (Unit: $ Billion)



AI-capable chips in PC (Unit: $ Billion)



1) AI-capable chip for low-end smartphone market is likely to be less than $0.3 Billion, thus not expressed in the graph. Premium category Includes flagship models.
Source: PwC analysis

Smartphones and PCs always have been high-end applications driving the demand for advanced chips using the advanced process. They must process vast amounts of data with low delay while maintaining portability, convenience (through a thin, lightweight design) and long battery life. As a result, the performance of APs—which integrate high-performance computing units like CPUs, GPUs, and ISPs—has been a key competitive factor in the smartphone and PC markets.

A growing trend further driving the device performance is the shift toward "edge AI." Previously, CPUs or GPUs handled these tasks, but as AI models become more complex and sensitive data increases, it has led to the adoption of NPUs within devices. An NPU, a dedicated AI processing core integrated within an AP/SoC, can enable faster, and more secure data processing. This trend is expected to fuel semiconductor market growth, particularly in premium product lines.

With faster, more secure NPUs and advanced on-device AI, smartphones and PCs can offer seamless AI experiences. Smartphones will likely be able to summarize calls in real time and enhance photos instantly without external apps. PCs can enable AI-driven noise cancellation for clearer video calls and provide real-time live caption translations without lag.

The demand for AI-enabled smartphones and PCs is already growing, and NPUs and edge AI may continue to drive the chip market forward in these industries.

Behind the AI PCs and smartphones

As processors advance, high-performance DRAM is essential for supporting faster data transfers and seamless processing. This need is further driven by on-device AI, where real-time AI processing demands efficient memory solutions that manage high data loads while preserving power efficiency.

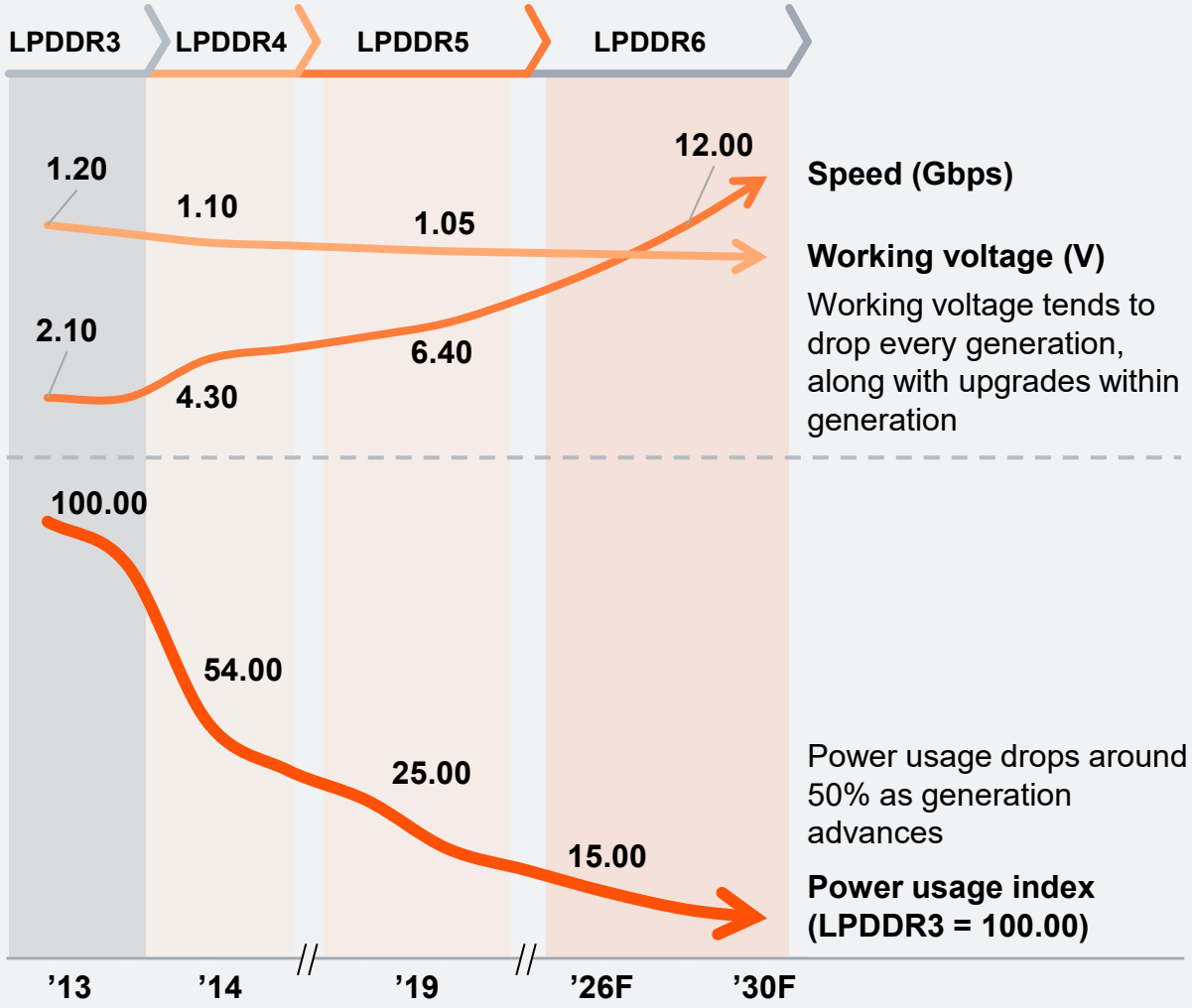
While HBM is synonymous with high-performance memory, its power limits its use in smartphones and PCs, where battery life is crucial.

LPDDR, or low-power double data rate DRAM addresses this challenge by balancing high-speed processing with high power efficiency, making it vital for next-generation smartphones and AI-driven computing.

Each LPDDR generation upgrade reduces power consumption by 30–40% through lower operating voltage, with design and process advancements adding 10–30% more savings within the generation. Whether it's a shift of generation or within the same group, the upgrade cycle is getting extended from 1-2 years to around 3 years. LPDDR 6 (expected in 2026) may achieve roughly 50% lower power consumption compared to LPDDR5, with additional improvements expected by 2030.

As AI workloads expand and energy efficiency remains a priority, LPDDR may continue to drive DRAM market growth, enabling high-performance, power-efficient computing in mobile and PC devices.

Relative power usage of LPDDR by generation



Source: Expert interview, PwC analysis

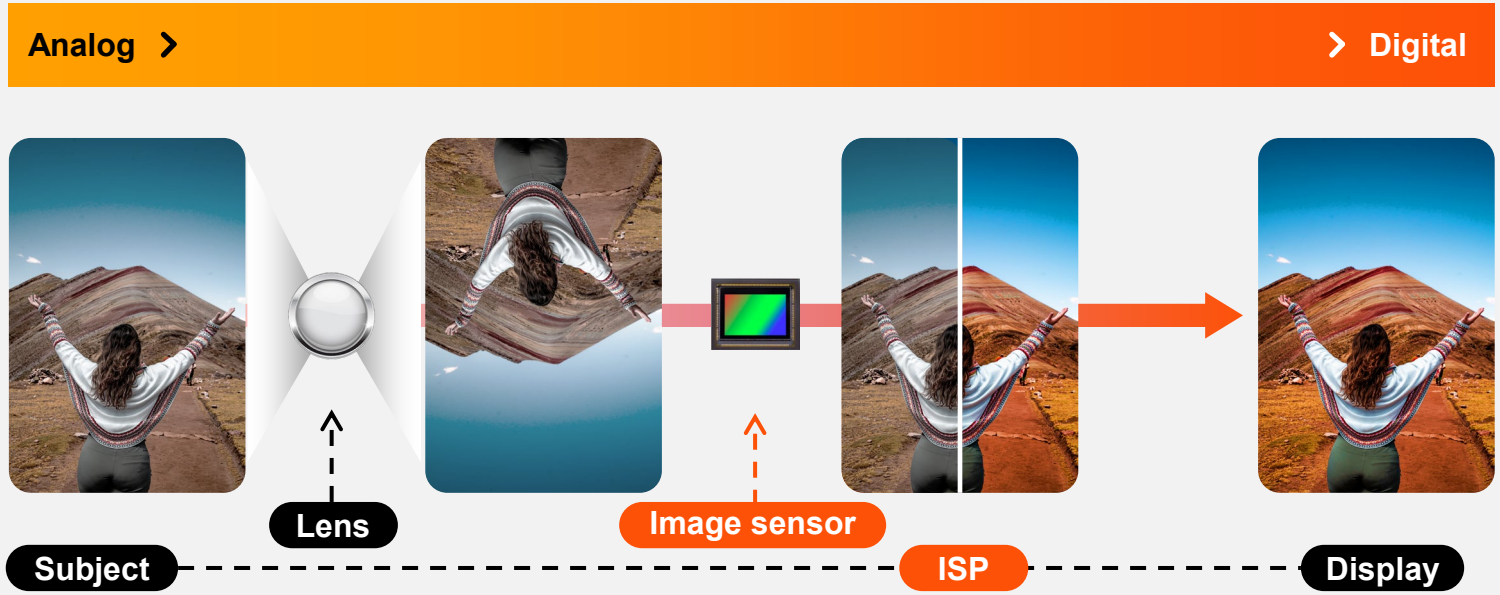
Turning an amateur into a pro: Image signal processors

Photography once demanded careful manual settings, but successive waves of automation—first in point-and-shoot film cameras, later in digital compacts, and now in smartphones—have made high-quality imaging effortless.

At the core of this process are the camera sensor and the ISP. The sensor functions like an “eye”, receiving light and converting it into electrical signals. ISPs act like the brain here, analyzing and processing those signals in real time to improve the final image. High-performance smartphone cameras rely on the synergy between high-resolution sensors, multiple lenses, and, most importantly, powerful ISPs.

As camera features become more advanced, consumer expectations for better photos are also rising. To meet this demand, smartphones now have multi-camera module setups - like triple or quad cameras and higher-resolution sensors, which in turn require ever-faster ISPs. Of course, the demand for lenses or higher pixel counts of camera sensors increases, but it is an ISP’s role to utilize these resources and bring high image quality to life.

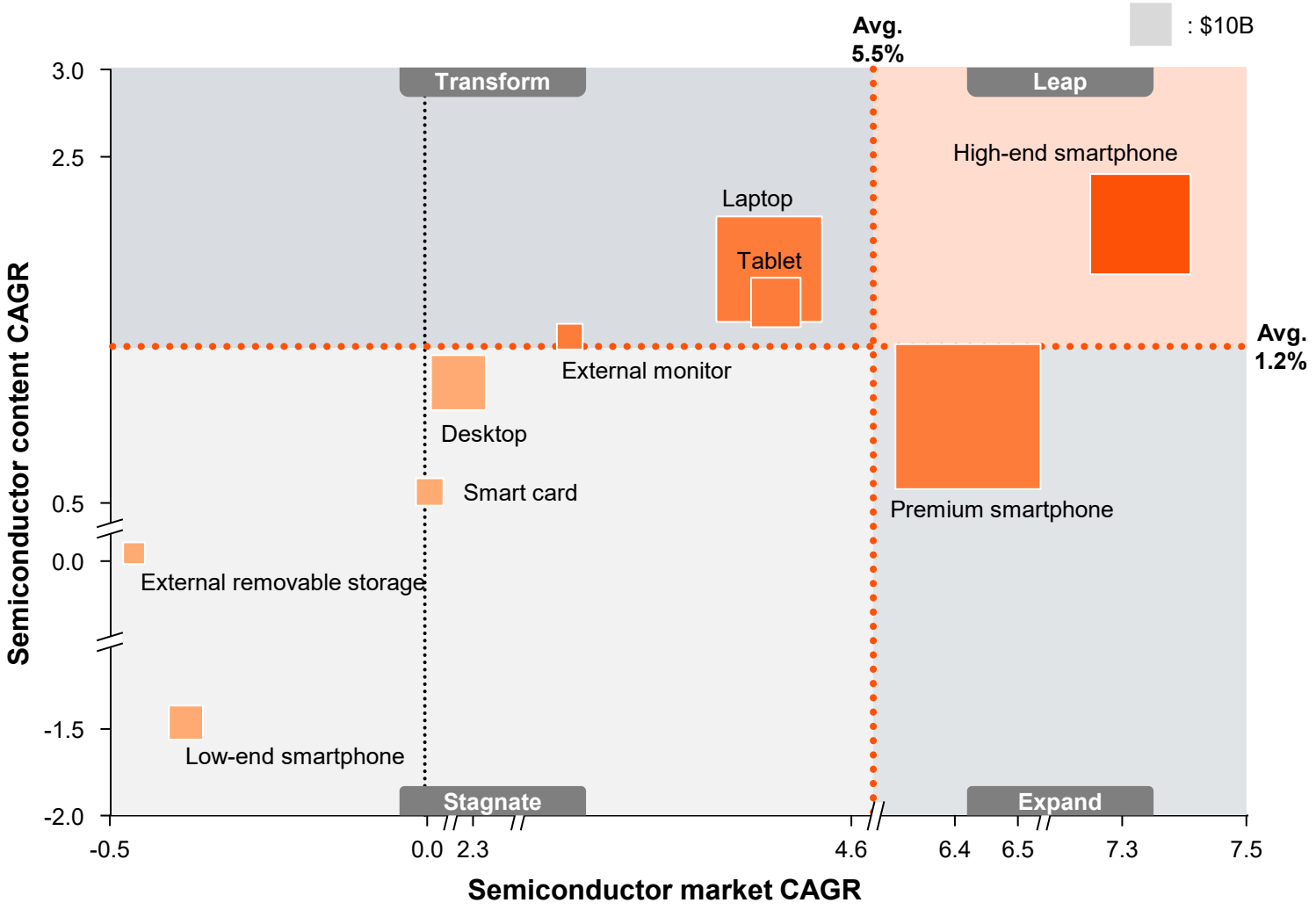
How images are processed with image sensors and ISPs



At the same time, shrinking bezels and growing display-to-body ratios leave less internal space, so stacked lenses, folded-periscope optics, and low-power ISP IP blocks become critical.

Consequently, advancements in miniature camera modules and highly advanced on-chip ISPs are emerging as a fresh growth driver for smartphone semiconductors, enabling future devices to capture professional-grade images from the palm of your hand.

Semiconductor demand by application, 2030



On-device AI

As smartphone functionalities continue to expand, smartphones are no longer just communication devices but are strengthening their position as computing devices. Moreover, smartphones are currently experiencing stronger semiconductor demand growth compared to other computing devices like PCs and laptops.

Among them, high-end smartphones, due to lower peripheral costs (such as camera lenses and displays) and relatively affordable prices compared to premiums, are experiencing strong demand. In contrast, the demand for low-ends is relatively weak.

Recently, as computing devices are increasingly equipped with AI functions, the proportion of semiconductor costs in COGSs is rapidly increasing, particularly in laptops and smartphones. The integration of AI functions is occurring more actively in laptops compared to desktops, resulting in a relatively larger increase in the proportion of semiconductor cost in laptops.

On the other hand, applications such as smart cards and external removable storage are showing relatively weak demand intensity.

Semiconductor demand intensity for applications by 2030

Applications			Demand intensity	Demand trends
Compute	PC	Desktop (S)		Although desktop-market growth has slowed, recent shifts towards high performance have increased the adoption of high-performance CPUs and GPUs.
		Laptop (T)		The trend is increasing for the integration of GPUs, CPUs, and display driver ICs due to the incorporation of AI functions and the expansion of high-resolution, refresh rate features.
	Smart-phones	Premium smartphone (E)		Despite the high performing APs, they are influenced more by modular components like display size and camera count than by semiconductors.
		High-end smartphone (L)		They offer similar levels of functionality as premium smartphones but are more affordable, providing fast connectivity, powerful AI, AR/VR integration, and top-tier memory features.
		Low-end smartphone (S)		They offer basic functions and cost efficiency with relatively fewer semiconductors, with affordable 5G, cost-effective SoCs, and cloud reliance for intensive tasks.
	Others	Tablet (T)		With significant advancements in AP and display performance compared to the past, demand remains stable, driven by portability.
		External monitor (T)		High-refresh gaming panels and dual monitor office setups drive up semiconductor content, including high-speed interface ICs and advanced driver and power ICs.
		Smart card (S)		Smart card unit growth is modest, but migration to contactless NFC variants sustains secure MCU shipments.
Storage	External removable storage	(S)		Cloud storage slows external drive demand, and mature NAND flash leaves little room for further chip growth.

Weak Strong

L Leap E Expand T Transform S Stagnate

Industrial

Semiconductors are helping to revolutionize a wide variety of industrial sectors. The accelerating shift toward renewable energy in response to climate risks, the growing need for medical innovation due to aging populations, and the rise of smart manufacturing in factories and farms is key examples of trends that are deeply connected with semiconductor advancements.

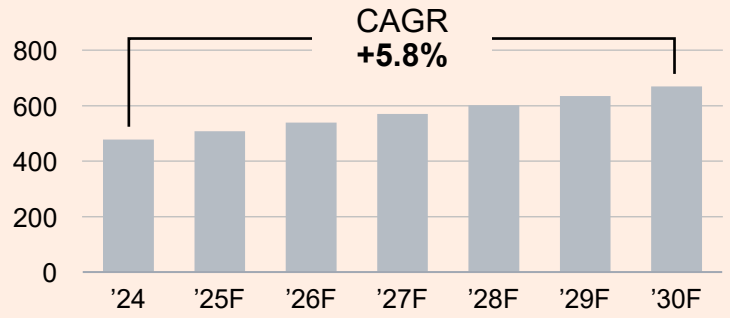
Semiconductors support healthcare professionals by enabling faster diagnoses, more efficient surgeries, and preventive care through advanced CPUs, GPUs, biosensors, and MEMS technologies. The transition to renewable energy can also fuel the demand for SiC power semiconductors, while the expansion of smart production across industries is driving the semiconductor market across sensors, connectivity ICs and AI chips.

As the industries continue to integrate intelligence, automation, and AI, semiconductors will likely penetrate ever more domains, driving efficiency and sparking further innovation.

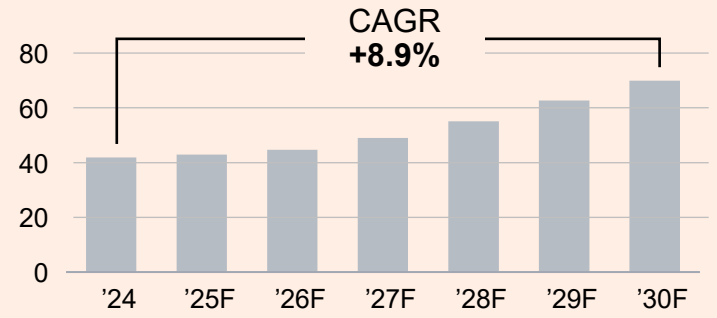
Industries never stop changing

Industries around the world—including healthcare, agriculture, manufacturing and defense—are constantly evolving, driven by global demographic shifts, productivity gains from new technologies, the emergence of new product categories, and climate related risks. Many of these forces are boosting demand for higher-performance semiconductors and greater volumes overall. By 2030, chips will likely be embedded in an ever-wider range of everyday applications.

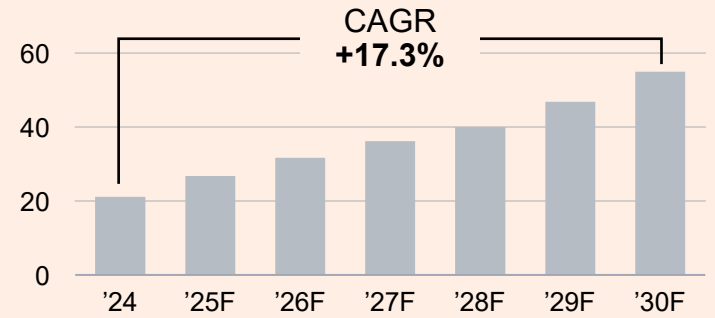
Medical device market (Unit: $ Billion)



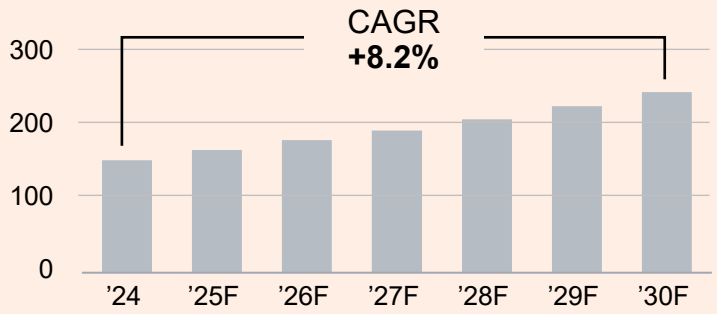
Automation equipment market



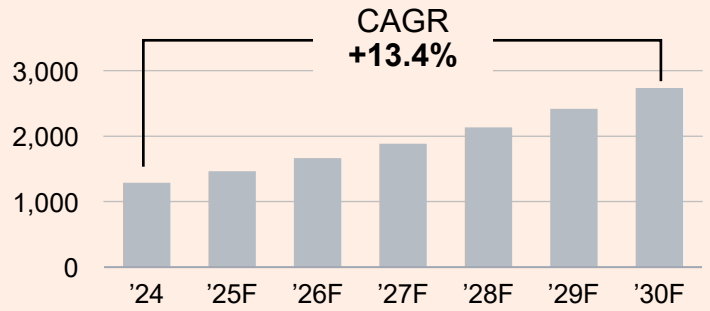
Smart agriculture equipment market



Defense equipment market



Renewable energy market



Source: IEA, Statista, Gartner, PwC analysis

Semiconductors at the heart of medical innovation

It is a worldwide trend that the population is aging, with a natural surge of interest in healthcare. Semiconductors play a vital role in medical innovation.

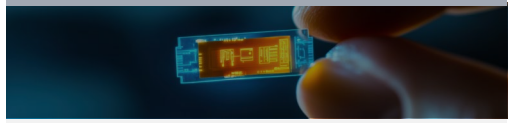
One notable example is robotic-assisted surgery, which is gaining more and more share. In the U.S., robotic-assisted ventral hernia repairs rose from 2.1% in 2010 to over 20% in 2020.[1)] This growth is powered by micro-electro-mechanical-systems (MEMS) technology, which yields sensors and actuators for precise movements while real-time GPU-powered analysis assists the surgeon's eyes

Diagnostics like CT, MRI, and 3D ultrasound, powered by GPUs, are evolving to reveal greater detail previously undetectable. Cloud/Edge AI tools, driven by CPUs, GPUs, and connectivity ICs, can further enhance diagnostic accuracy and efficiency. Beyond physical hospitals, semiconductors can also enable the possibility of remote diagnostics and patient monitoring through biosensors, AI analytics, and post-treatment-care robots equipped with sensors, MCUs, and communication ICs.

Some semiconductors should obtain certifications by passing tests for electrical safety and electromagnetic compatibility (EMC) or should be manufactured with the idea of going through these tests as a device. While it's a field with relatively strong regulations, it seems like there is ample opportunity in the medical field for chipmakers, from MEMS to AI accelerators, GPUs and a lot more.

Semiconductors in future medical service area

Personal testing



Advanced biosensors with signal processing units

Telemedicine service

Communication ICs and Bio Sensors

Diagnostic equipment

High-performance GPU, CPU, signal processors and communication ICs

Robotic surgery

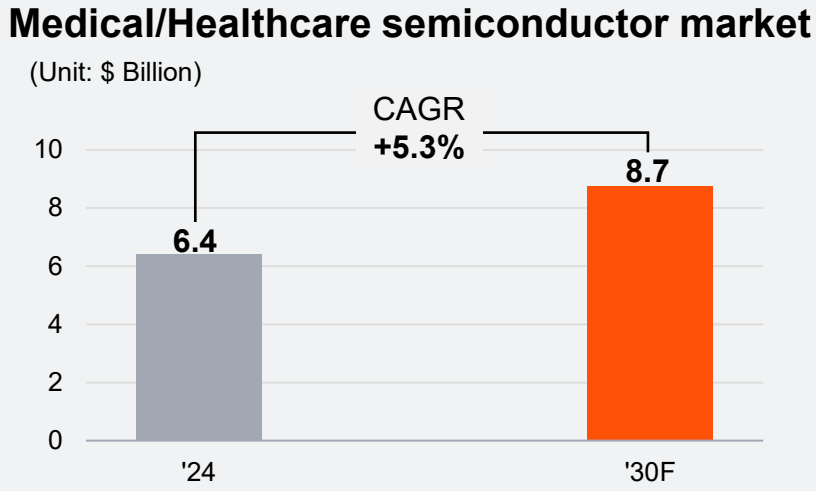
AI-powered vision processing chips and MEMS-based motion sensors and controller units

Miniature surgical robots

MEMS-based implants such as artificial medical devices

Post-surgical monitoring

Biosensors, communication ICs, MCUs



1) Brian T Fry, Surgical Approach and Long-Term Recurrence After Ventral Hernia Repair", 2024
Source: PwC analysis

Transitioning to renewable energy

With increasing global attention on the climate crisis, the global solar PV and wind capacity climbed from 900 GW in 2016 to over 2,000 GW in 2023. This change is accelerating, and the total capacity in 2030 is expected to reach 5,500 GW. According to IEA, Solar photovoltaic (PV) and wind energy are expected to supply well over 90 % of the incremental renewable capacity as they are the most accessible and rapidly expanding renewable sources.

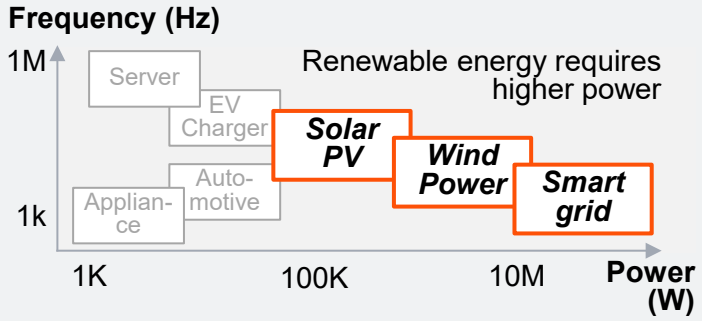
Both solar and wind power rely heavily on semiconductors to enable effective power transmission and usage. Solar energy, generated as direct current (DC), must be converted to alternating current (AC) for grid compatibility. Additionally, due to the variability in sunlight and wind speed, semiconductors play a crucial role in stabilizing electrical output from renewable sources.

For stable and efficient power transmission, energy sector especially demands semiconductors that can survive a high-voltage environment compared to other applications, making silicon carbide (SiC) critical.

As renewable energy adoption expands, smart grids and energy storage systems (ESS) are rising as well. They enable a stable supply of renewable energy by storing excess electricity and redistributing it when production dips. To enable this, smart grids require continuous power monitoring, leading to increased demand for communication ICs throughout the grid and CPU/GPUs at central control stations. ESS, acting as backup batteries, also relies on inverters, converters with power semiconductors, and battery management system (BMS).

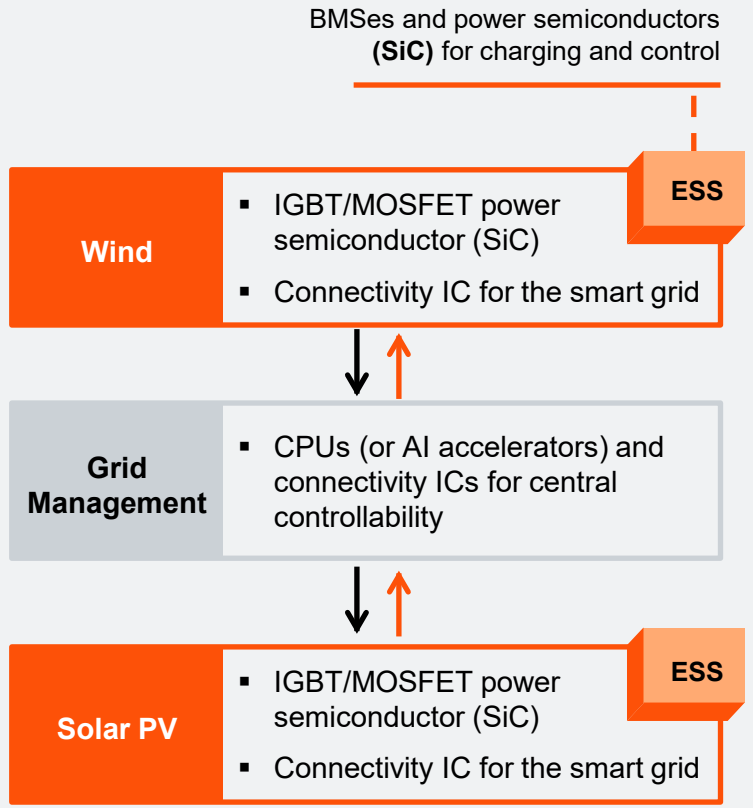
As the use of renewable energy continues to grow over time, growth in demand for power semiconductors is inevitable.

Energy requirements by application



Source: Infineon, PwC analysis

Semiconductor needs in renewable energy market



Smart production evolution continues

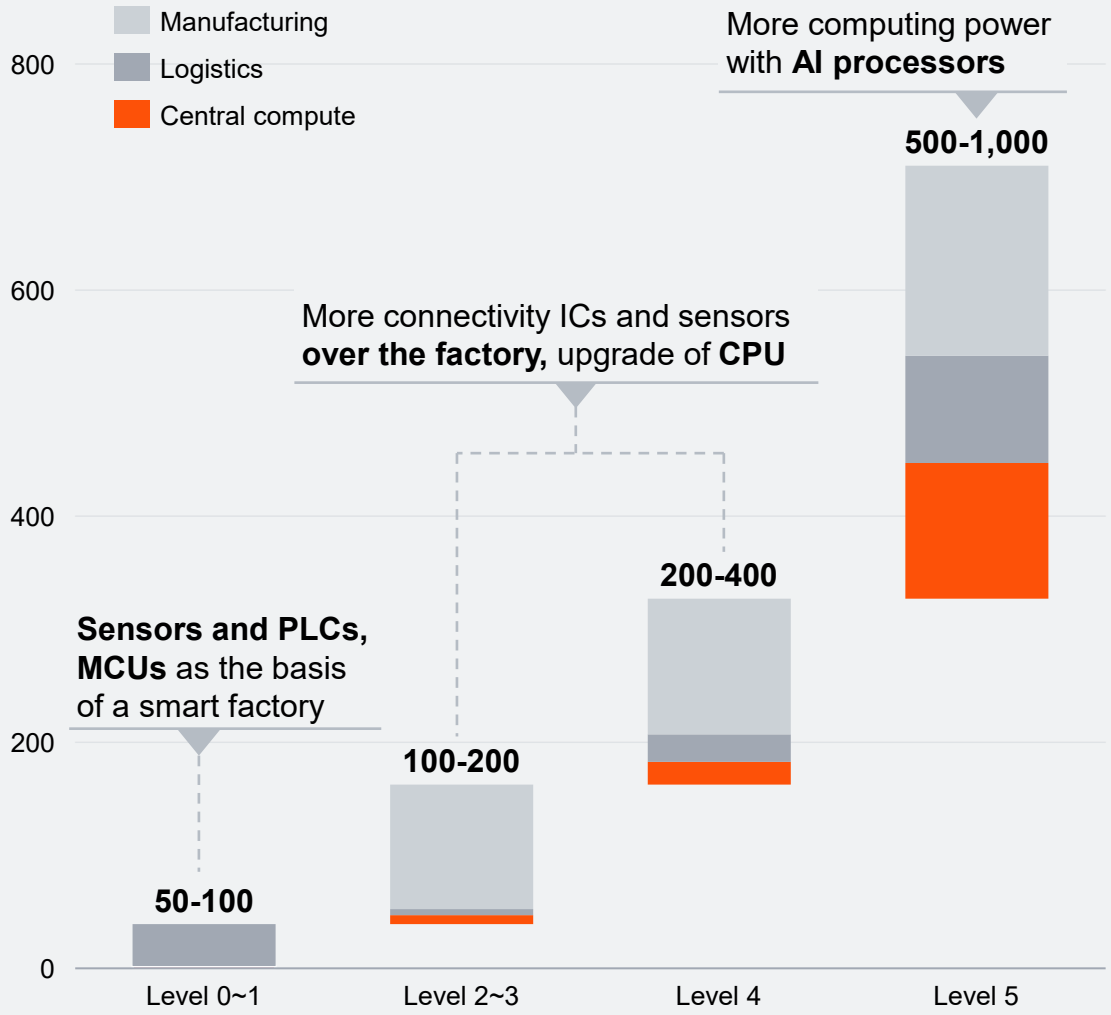
With rising labor costs and a shrinking workforce, smart factories, which improve the entire production and logistics with AI and IoT, are expanding rapidly. They rely heavily on semiconductors to enable automation. Connectivity ICs enable IoT equipment throughout the factory for real-time tracking of raw materials to inventory. Industrial computers (programmable logic controllers, or PLCs) use ASICs or CPUs to remotely control the equipment. Sensors, MCUs, and MEMS devices can help detect any defects and conduct precise machinery control. And PMICs help keep these systems power-efficient. If we try to define the level of automation based on automation pyramid, right now, companies are moving from level 0-1 to level 2-3, and even level 4 and 5 to improve efficiency. With the wave of fully automated factories, we may be able to see more demand on computing power and connectivity ICs in industry.

Furthermore, the demand for automated, smart production applies not only to mass production in factories, but also to smart agriculture and smart aquaculture. In smart farms, sensors monitor environmental conditions, transmitting data to AI processors that improve crop growth. Automated machinery, guided by GPS, MCUs, and CPUs, performs planting and harvesting. Smart aquaculture follows a similar model, with water quality probes, machine-vision fish counters and AI-controlled feeding robots to boost efficiency and sustainability of the farm.

As automation advances, the demand for high-performance semiconductors can grow, making industries more intelligent, data-driven, and self-sustaining.

Semiconductor content by automation levels[1)]

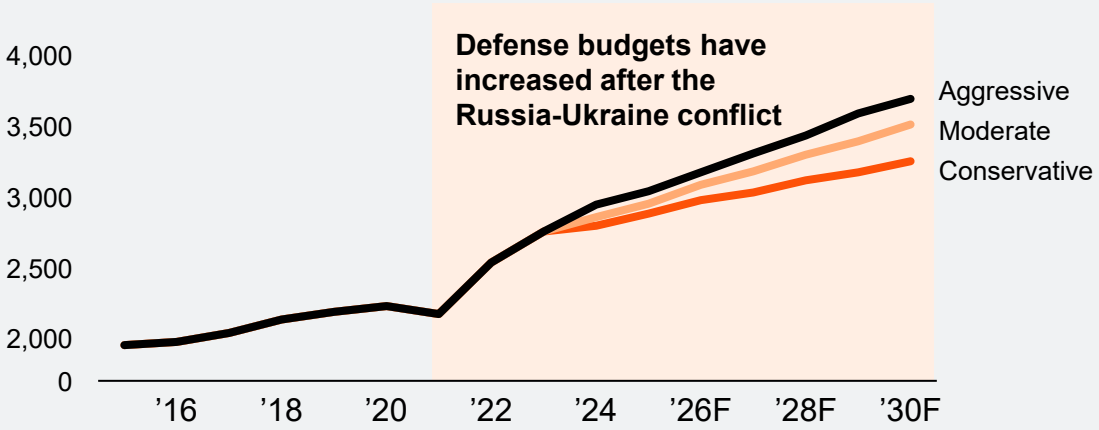
(Unit: $ Thousand)



1) The value of semiconductor was estimated based on 10,000m^2 factory producing automotive parts with a very simple production line, it must vary based on the industry, factory's size and the value of semiconductors. Lv.0-1 is a basic automation of device with PLC, Lv.2-3 is a partial automation of whole factory based on data, Lv.4 leverages enterprise-level data for automation, and Lv.5 is total automation, self-improving the performance through AI. The numbers are only intended to illustrate the trend of the increased value of semiconductors as the automation level increases.
Source: PwC analysis

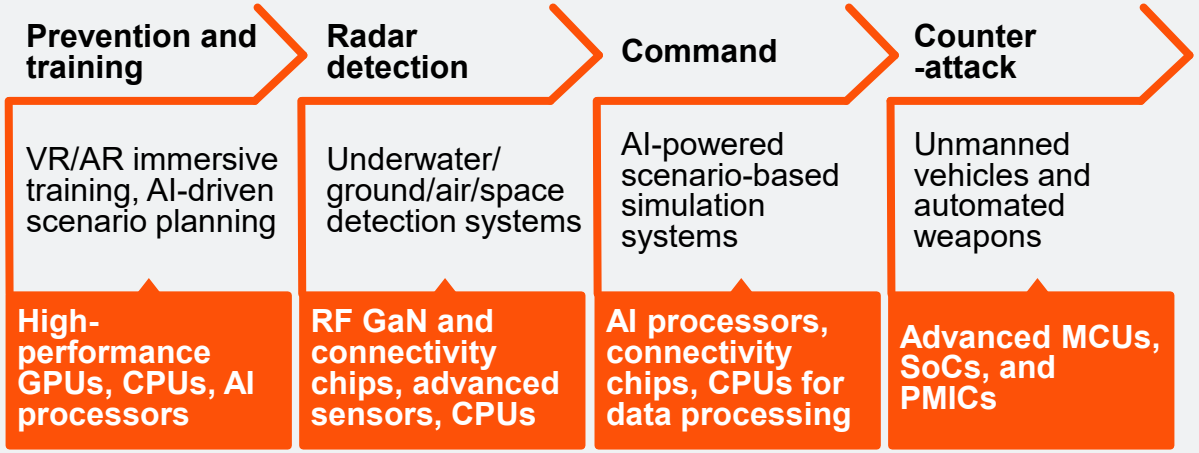
Advanced defense system needs advanced chips

Global defense budget (Unit: $ Billion)



Source: KIET

Flow of defense and semiconductor

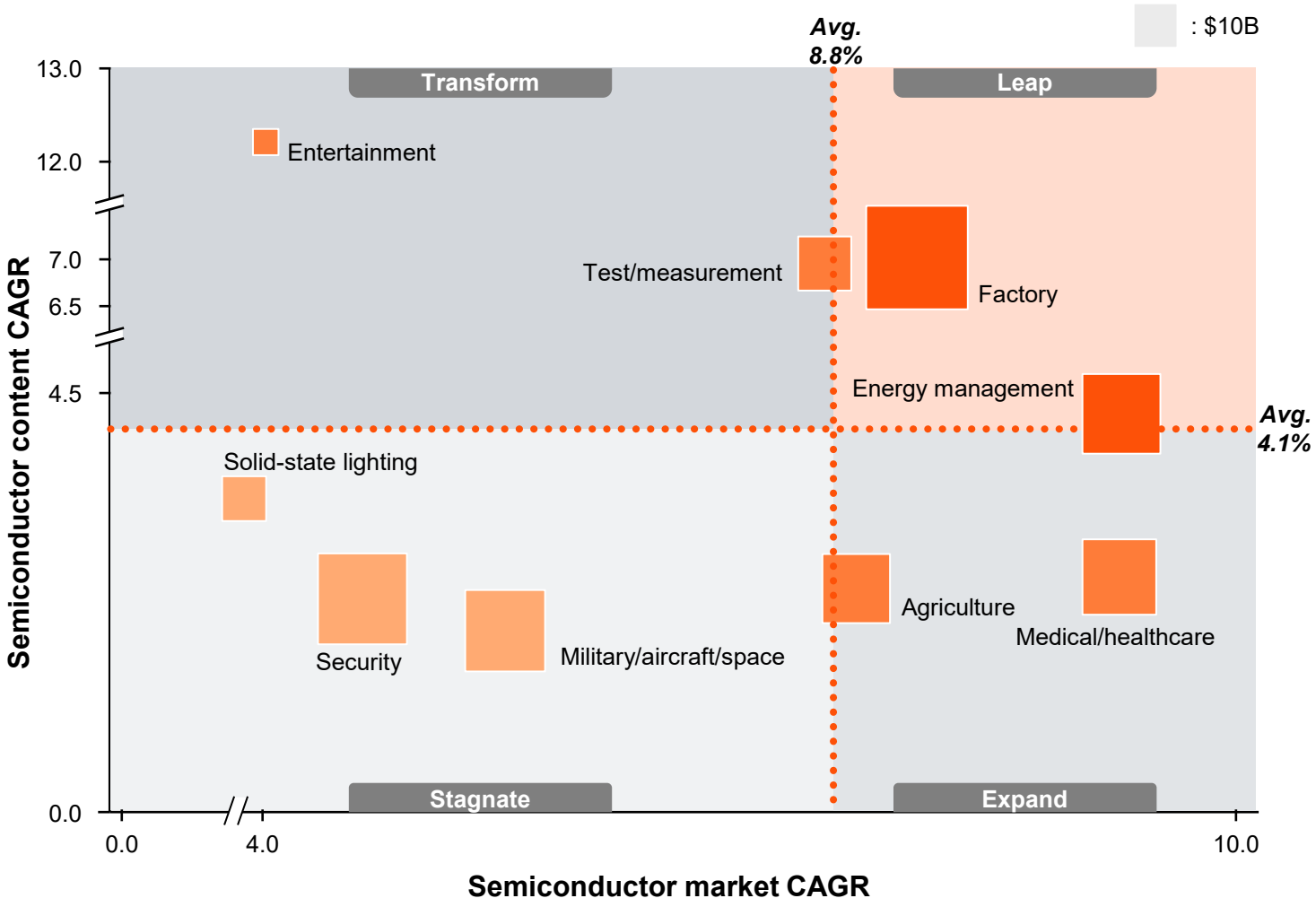


As geopolitical tensions and security threats rise, global defense budgets are increasing. From 2015 to 2022, the average defense budget was around $2 trillion, but this figure is expected to reach $3 to $4 trillion by 2030. This budget increase is being allocated not just to traditional military buildup but also towards higher-level technological innovations, unmanned systems, and advanced warfare technology. To reduce human casualties and improve mission success rates, rapid advancements are being made in drones, unmanned ships, and fighter jets.

Defense systems are structured around key stages: prevention and training, radar detection, command, and counterattack. Now, real-time detection system, combined with machine learning and VR/AR devices are backing concrete defense strategies. In terms of command, software-defined defense, with AI-based data analysis and real-time decision support are being rapidly adopted given the industry's need for quick decision-making. High security levels are demanded, leading to growth in semiconductors embedded with security and encryption software to help prevent cyber attacks.

In combat scenarios, devices can now be connected to the command room, some even activated with edge AI chips. Semiconductors used in combat situations also require high reliability and durability, and thus packaging materials such as ceramic may be used for high-radiation environments and to enable long lifetime. High-performance GaN RF chips, known for efficiency, durability, and speed, are also projected to see increased demand. As technology continues to evolve towards unmanned and advanced defense, semiconductors will likely remain a crucial strategic asset in the defense market.

Semiconductor demand by application, 2030



Automation and transition

Smart factories are poised for expansion, leading to increased growth in production machinery and control infrastructures, particularly focusing on upgrading microcontroller units (MCUs). Concurrently, the growing renewable energy sector is also set to boost demand for high-voltage power semiconductors.

Moving forward, active integration of robots into production is set to amplify the need for semiconductors, especially in test, measurement, and automation processes, which are vital for enhancing production efficiency. Additionally, the application of AI in the medical and healthcare sectors is expected to drive higher semiconductor content rates.

In contrast, the military and security industries rely on customized semiconductors, leading to fragmented demand. Meanwhile, solid-state lighting, part of a large consumer market, is nearing maturity as LED lighting has achieved significant penetration, resulting in lower future growth compared to other industries.

Semiconductor demand intensity for applications by 2030

Applications		Demand intensity	Demand trends
Industrial electronics	Security (S)		In CCTV, edge AI for object detection is moving into the camera itself, lifting demand for on-sensor ISPs, NPUs and low-power DRAM.
	Factory (L)		The acceleration of digitalization and automation in industrial sites, along with the expansion of smart factories, is leading to increased integration of sensors, MCU/MPUs, and power chips.
	Medical/healthcare (E)		Advanced imaging and edge diagnostics add GPU servers on the back-end, while on-device DSP/FPGA and ASICs grow slowly due to stringent certification cycles.
	Energy management (L)		Improving energy efficiency and stricter carbon regulations are accelerating the transition to renewable energy and increasing the use of power chips to control the high power.
	Solid-state lighting (S)		General lighting is mature, but mini/micro LED, smart lighting and horticultural fixtures lift demand for advanced LED driver ICs, wireless MCUs and sensors.
	Test/measurement (T)		As factory automation advances, quality control automation is also expanding, driving increased demand for various sensor semiconductors.
	Entertainment (T)		In the cruise and casino markets, increasing demand for AI and high-resolution/multiplayer capabilities is driving greater integration of GPUs and memory.
	Agriculture (E)		Despite limited cost share in machinery-centric agriculture, smart farming is accelerating demand for sensors, driving strong semiconductor market growth.
Others	Military/aircraft/space (S)		The aerospace-related downstream market is growing; however, as it is a market where reliability is crucial, node migration is slower, driven more by value per chip than by volume.
		Weak — Strong	

L Leap E Expand T Transform S Stagnate

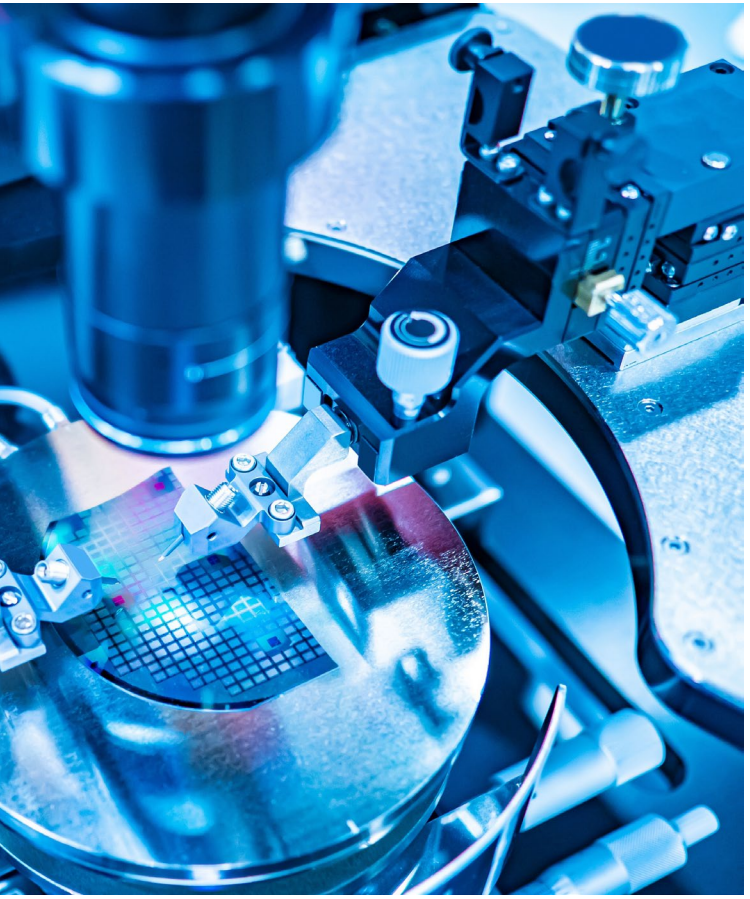
3

Supply Analysis

The race for semiconductor supremacy

Why supply matters?

The semiconductor supply chain is encountering escalating complexity and volatility driven by geopolitical factors, localization, and heightened customer expectations. This section explores market trends and technological advancements, assessing their impact on the future disruption and resilience of the supply chain.



Design

Defining chip function and circuit design

Fabrication

Forming chip's core structure at wafer level

Packaging and Testing

Interconnecting and packaging chips in usable form and testing

IP and EDA

IP

Reusable design components to reduce development time

EDA

Software tools to automate design processes

Equipment and Material

Equipment

Machines used in semiconductor manufacturing, like EUV lithography

Material

Essential substances for chip fabrication, including wafers, chemicals, and gases

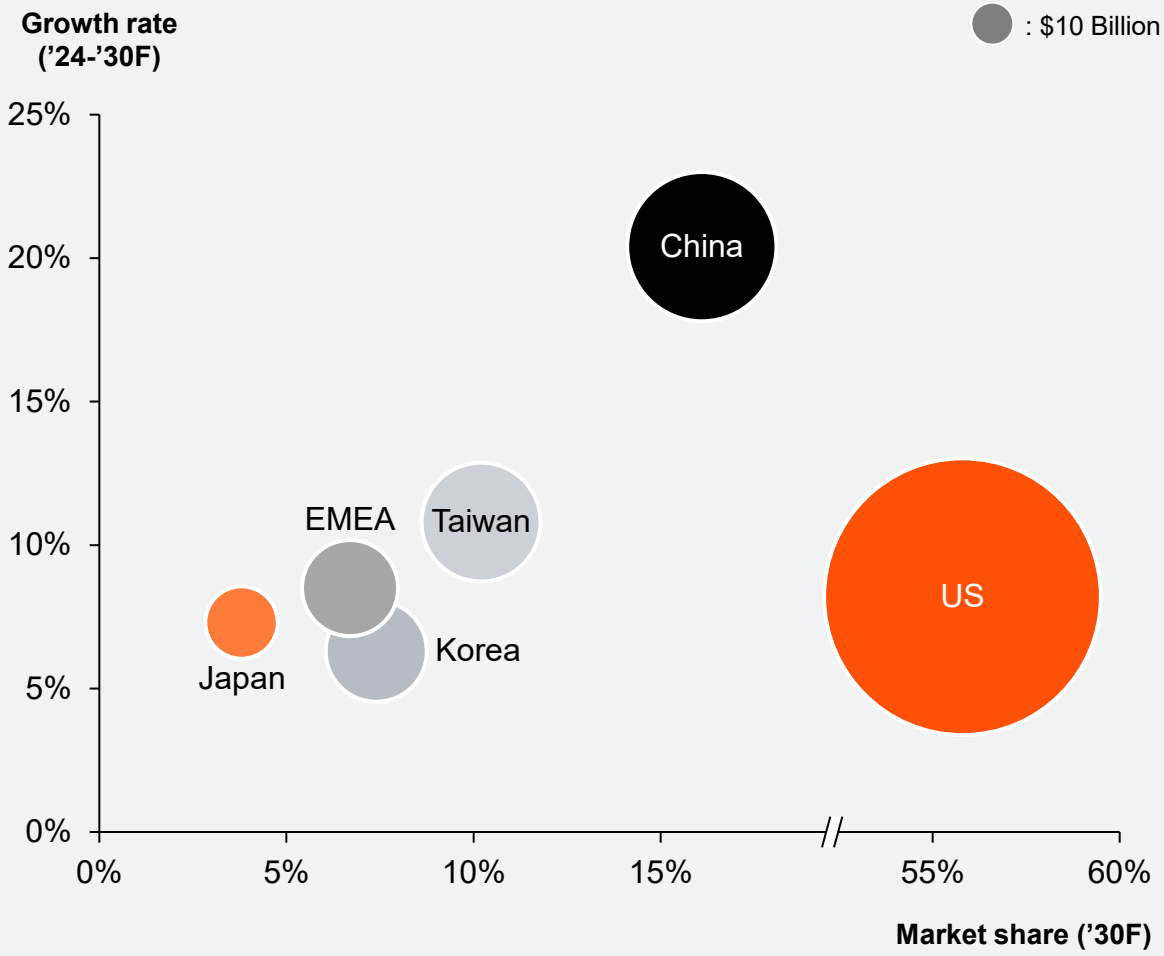
Design, IP and EDA

With the growth of the global semiconductor design market, substantial investments are being made worldwide, intensifying competition in the field. As design complexity increases at advanced process nodes, the costs associated with IP licensing and EDA tool usage have risen sharply, making cost reduction a critical competitive factor.

Recently, there has been a notable shift from general-purpose chips to application-specific semiconductors, accompanied by a growing emphasis on low-power consumption and thermal management. Despite these challenges, design innovation remains the core driver of semiconductor performance improvements.

Close collaboration among fabless companies, foundries, and IP vendors—along with ongoing investment in specialized architectures—is expected to drive further market growth. Ultimately, these efforts can contribute to the advancement of the entire semiconductor ecosystem.

Global semiconductor design market[1)]



1) The above market forecast is based on analysis of major regions and includes the fabless market and a portion of IDM revenue attributed to chip design
2) PwC analysis based on major companies' annual report, estimated average revenue per design engineer
Source: PwC analysis

Where semiconductor leadership begins

The semiconductor industry stands at the forefront of the global race for technological supremacy, with each region making massive investments to reinforce its semiconductor ecosystem. Semiconductor design is receiving heightened attention for determining product value and differentiation, particularly in high-end markets like AI, data centers, and autonomous vehicles.

Chip performance extends beyond advanced process technology. Factors such as power efficiency, safety, and functionality hinge on the design stage, prompting territories to adopt specialized strategies. The United States concentrates on AI and HPC, China fosters broad in-house capabilities for self-sufficiency, Europe pursues leadership in areas like wide-bandgap power chips, Japan focuses on automotive semiconductors and image sensors, and Korea combines memory and foundry strengths with design expertise to explore emerging applications in mobile, AI, and automotive.

Securing a skilled semiconductor design workforce remains a pressing issue. By 2030, over 300,000 engineers may be required, yet the current figure is around 200,000.[2)] Because engineers need advanced competencies, quickly expanding this talent pool is challenging. Strengthening EDA tools, IP infrastructure, and training initiatives therefore can be crucial for a stable design ecosystem. By balancing cooperation and competition across regions and companies, design-led innovation can be a key driver in reshaping the semiconductor landscape.

Entering the era of custom ICs

Logic semiconductors are generally categorized into two categories: General-purpose and application-specific chips. General-purpose chip is designed to handle a broad range of tasks, these chips offer flexibility in supporting various workloads and software updates. However, this versatility often comes at a cost since general-purpose chips lack the specialized efficiency needed for highly specialized computing functions.

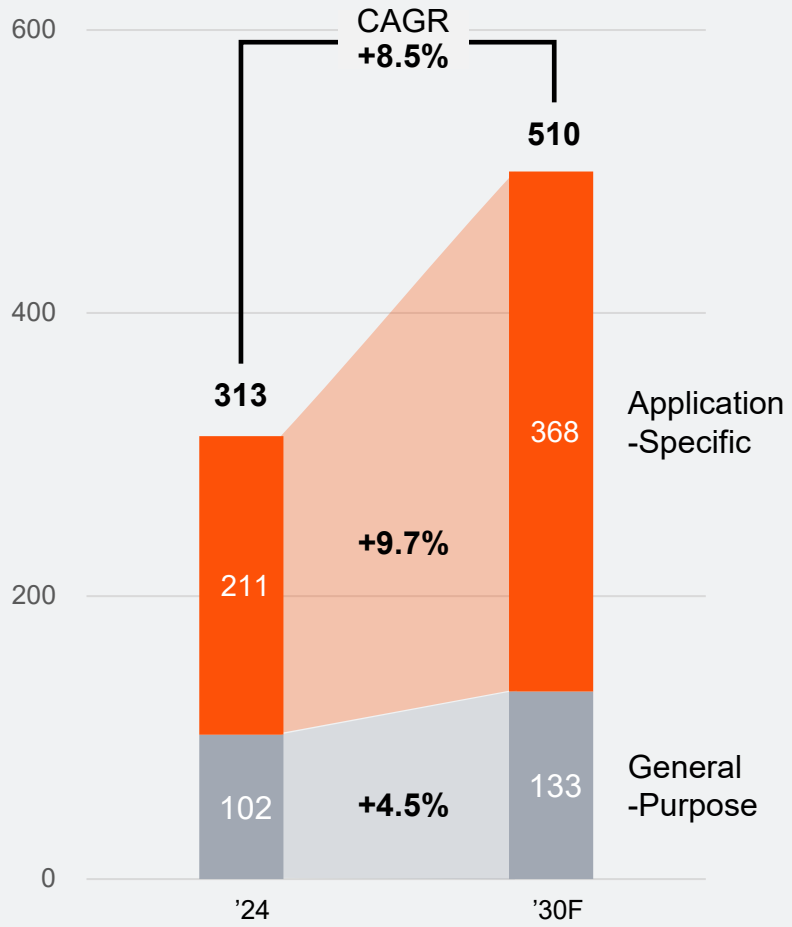
This is where application-specific chips come into play. Over time, these chips have gained traction to bridge the performance gap of general-purpose chips. While they offer less flexibility, they are purpose-built to meet specific requirements, delivering superior performance, power efficiency, and reliability compared to their general-purpose counterparts.

A deeper look into the application-specific category reveals two key segments: ASSPs and ASICs. ASSPs are tailored for a broader market segment or domain use, whereas ASICs are highly customized chips typically designed for a specific product or limited customer set.

The high costs and overspecification concerns in ASSPs have driven demand for ASICs. However, given the highly customized nature of ASICs that restrict their applications, securing cost competitiveness through sufficient production volume has become an enduring challenge. As ASIC developments advance, the demand for customized design architectures may increase, in turn creating a virtuous cycle for ASICs to gain price competitiveness and continue growth.

Global logic semiconductor market

(Unit: $ Billion)



Source: Omdia, PwC analysis

Balancing performance and power

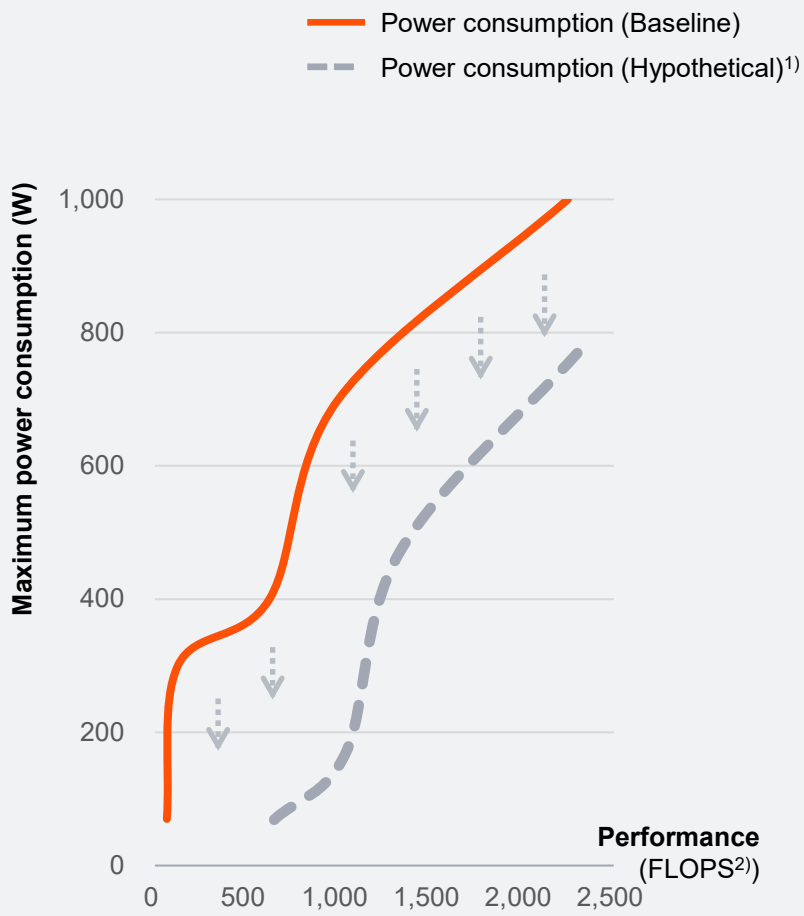
For years, semiconductor engineers have balanced performance, power efficiency, and area—the classic 'P-P-A' triangle. But as processors become faster and operate at higher voltages, their power consumption rises dramatically, generating more heat and using more electricity. In large data centers, this extra power leads to significant costs. Not only do faster chips demand more energy, but the cooling systems needed to remove the excess heat also consume a great deal of power—sometimes costing as much as the new equipment itself.

Process scaling adds another challenge. Advanced nodes place far more transistors on the same piece of silicon. Each switch is more efficient on its own, but the sheer density pushes total watts per square millimeter higher and creates hot spots. If those hot spots are not controlled, transistor mobility falls, timing margins shrink, and in extreme cases, permanent damage can occur.

These realities are forcing chip design companies to improve performance per watt instead of sheer peak numbers. Techniques such as dynamic voltage-frequency scaling, chiplet partitioning, and AI-assisted thermal management are becoming mainstream. Many companies now willingly trade a few percentage points of headline speed for substantial drops in power draw and operating temperature.

Looking ahead, R&D roadmaps point to architectures that target high compute throughput and low energy simultaneously—think specialized accelerators that wake only for specific tasks, or heterogeneous cores that shift workloads to the most efficient engine in real time. Such innovations address immediate user concerns—energy cost, battery life, sustainability—while keeping the door open to continued performance gains. In short, the industry is redefining “faster” to mean “faster and cooler,” ensuring that progress remains sustainable both technically and economically.

Data center GPU power consumption



1) The average power consumption of GPUs is expected to decrease in the long term, driven by architectural advancements, AI model optimization, and stricter energy regulations.
2) FLOPS(Floating Point Operation per Second: A measure of floating-point computations used as a performance metric for high-performance computers.
Source: PwC analysis

The unsung heroes powering the future of design

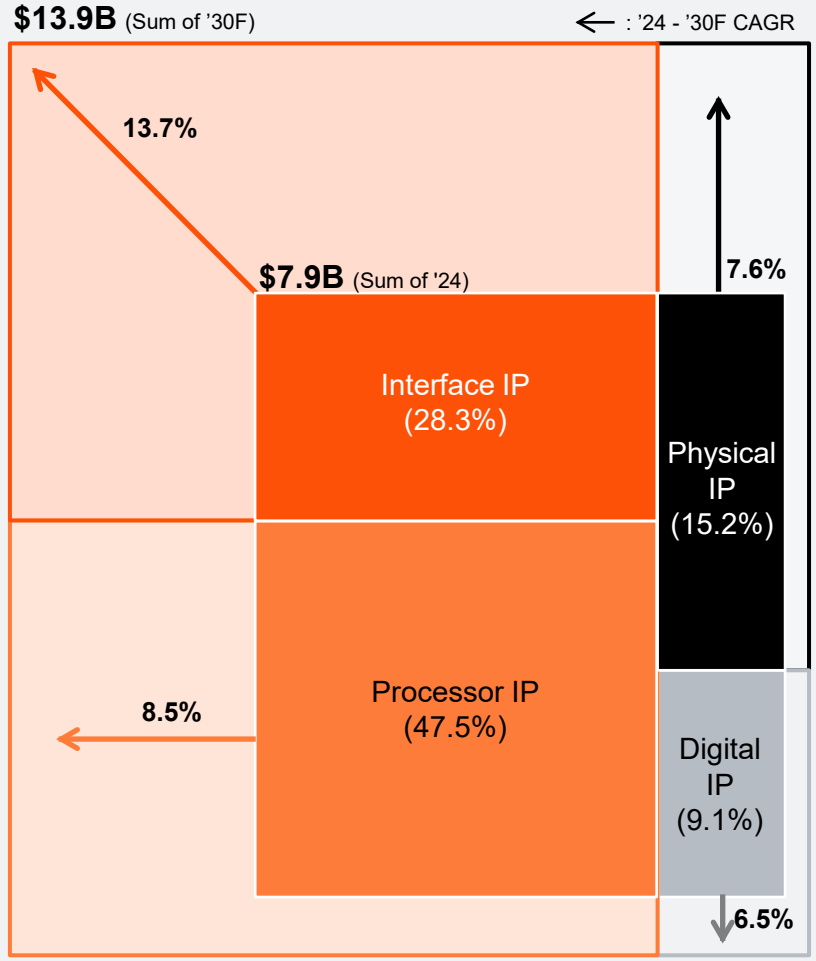
Semiconductor IP refers to the intellectual property related to semiconductor design, essentially meaning pre-designed blocks. As designs become more advanced, the need for a wide variety of blocks increases, which in turn highlights the importance of pre-designed semiconductor IP.

Among the various types of IP, interface IP and processor IP are attracting the most attention in terms of market size and growth rate. Interface IP is responsible for data exchange and connectivity between semiconductor chips. Its role is continually expanding in AI and autonomous vehicles, which require real-time processing and large-scale data transfers. As a result, interface IP is projected to experience the highest growth rate, given its critical function in enhancing performance.

Processor IP manages a system's control and computation. CPUs, MCUs, and similar cores belong to this category, which dominates the market since they appear in high-value chips for smartphones, servers, and more. As multicore and parallel computing proliferate, processor IP becomes increasingly vital to meet both high-performance and low-power requirements.

Put together, these IP blocks act like block pieces for silicon, letting fabless firms focus on system-level differentiation while reducing months of design cycles and millions of non-recurring engineering costs. As advanced packaging, low-power targets and domain-specific acceleration reshape product roadmaps, high-quality interface and processor IP can be the power that keep Moore's Law innovation moving forward.

Global semiconductor IP market



Source: PwC analysis

Soaring chip design costs: How can we contain the bill?

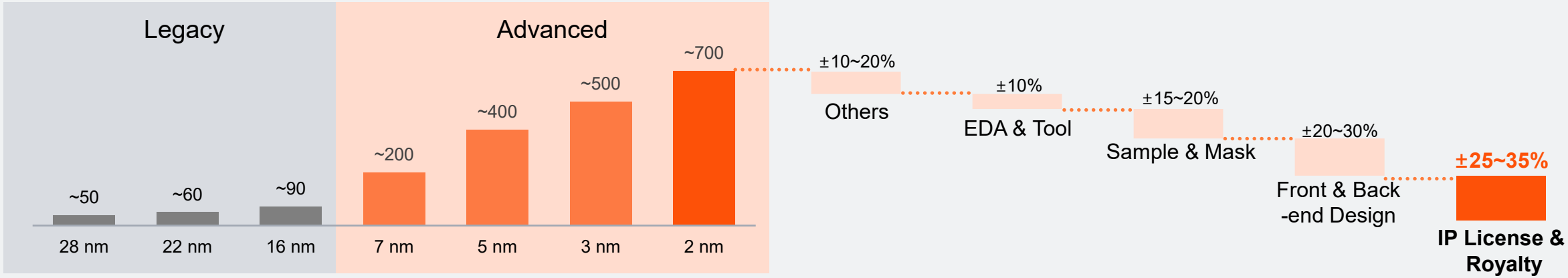
As semiconductor technology advances, chip design complexity drives up development costs. Meeting high-performance, low-power, and high-density demands in smartphones, data centers, and AI requires efficient integration of multiple functions, making semiconductor IP crucial. Pre-designed IP blocks like CPUs, GPUs, and AI accelerators reduce development time and enhance performance. However, moving to advanced nodes drives IP development and verification costs exponentially higher, increasing financial pressure.

In a market where advanced IP is critical for competitiveness, IP license & royalty can swallow 25–35% of industry leading project's budget.

To keep chip designs cost-effective, companies can: (1) Build reusable in-house IP, (2) Use chiplets and multi-node partitioning so only hot logic uses advanced nodes, (3) Adopt open-source like RISC-V to cut royalties, and (4) Strengthen cloud collaboration with EDA and foundries to catch issues early and avoid re-spins.

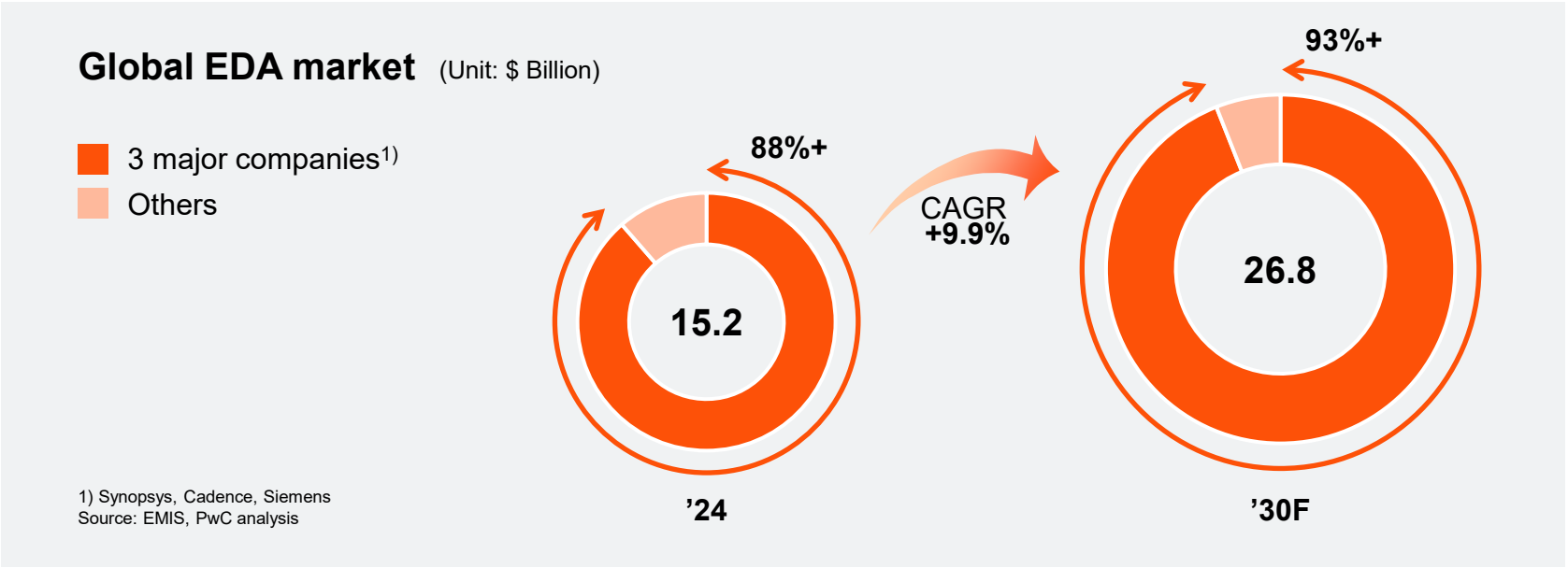
Balancing these levers can be essential for hitting aggressive power-performance targets without letting design budgets spiral out of control, enabling that innovation at advanced nodes remains both technically and economically sustainable.

Cost of chip design (Unit: $ Million)



Source: Expert interview, PwC analysis

Driving EDA innovation through mergers and acquisitions



Electronic Design Automation (EDA) tools let chip engineers model, verify and enhance their designs before a single mask set is written, slashing the risk of costly re-spins and steering layouts toward higher yield. As SoCs race to 2 nm and beyond, these platforms—now infused with AI for test-bench generation, anomaly detection, and place-and-route—are becoming even more critical, with the potential to cut design schedules by tens of percent this decade.

EDA market leadership remains highly concentrated. Established vendors enjoy two structural advantages.

First, proven reliability matters: because missed defects can wipe out a tape-out budget, design houses prefer suppliers with long track records and silicon-proven sign-off flows. Second, steep technology barriers protect incumbents: the big three have spent billions of dollars on R&D and have rolled up hundreds of niche tools through systematic M&A.

Going forward, the depth of proprietary datasets used to train AI-based EDA tools is expected to become a key competitive edge, and major players are already acquiring start-ups both for innovative algorithms and for the data that powers them.

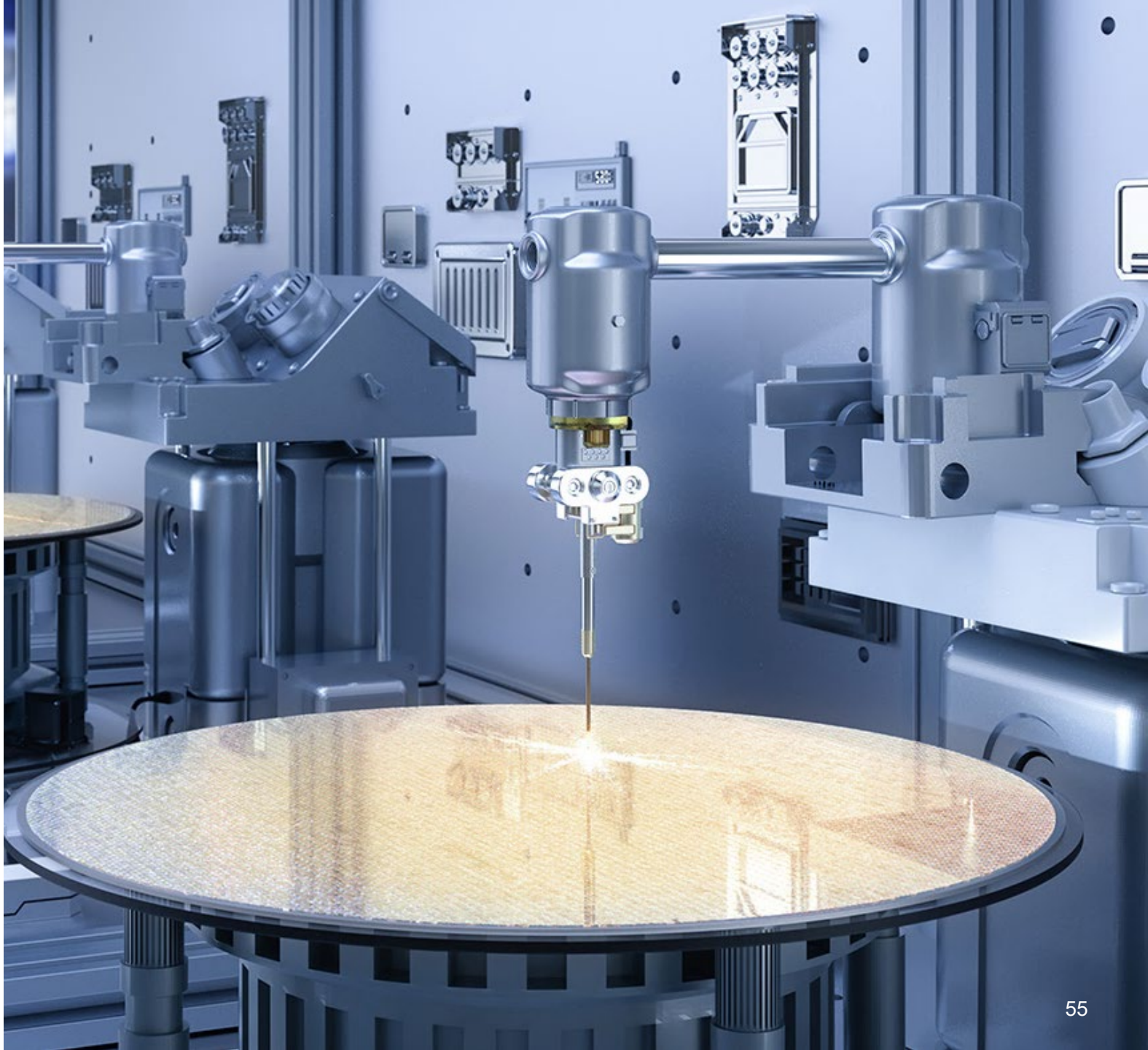
For chipmakers, a concentrated supplier base can mean higher license fees, yet the productivity gains often outweigh the premium. Rather than hoping for a surge of new EDA entrants, most customers are likely to focus on forging tighter partnerships, adopting cloud-based tool flows, and developing in-house automation scripts to squeeze more value from the ecosystem that now underpins a lot of the advanced semiconductor projects.

Fabrication

Across the front-end manufacturing sector, new fab construction is under way in multiple regions. This trend of investment has accelerated under the influence of government subsidies and the needs to stabilize supply chains, as companies simultaneously pursue large-scale facility investments and technological advancements.

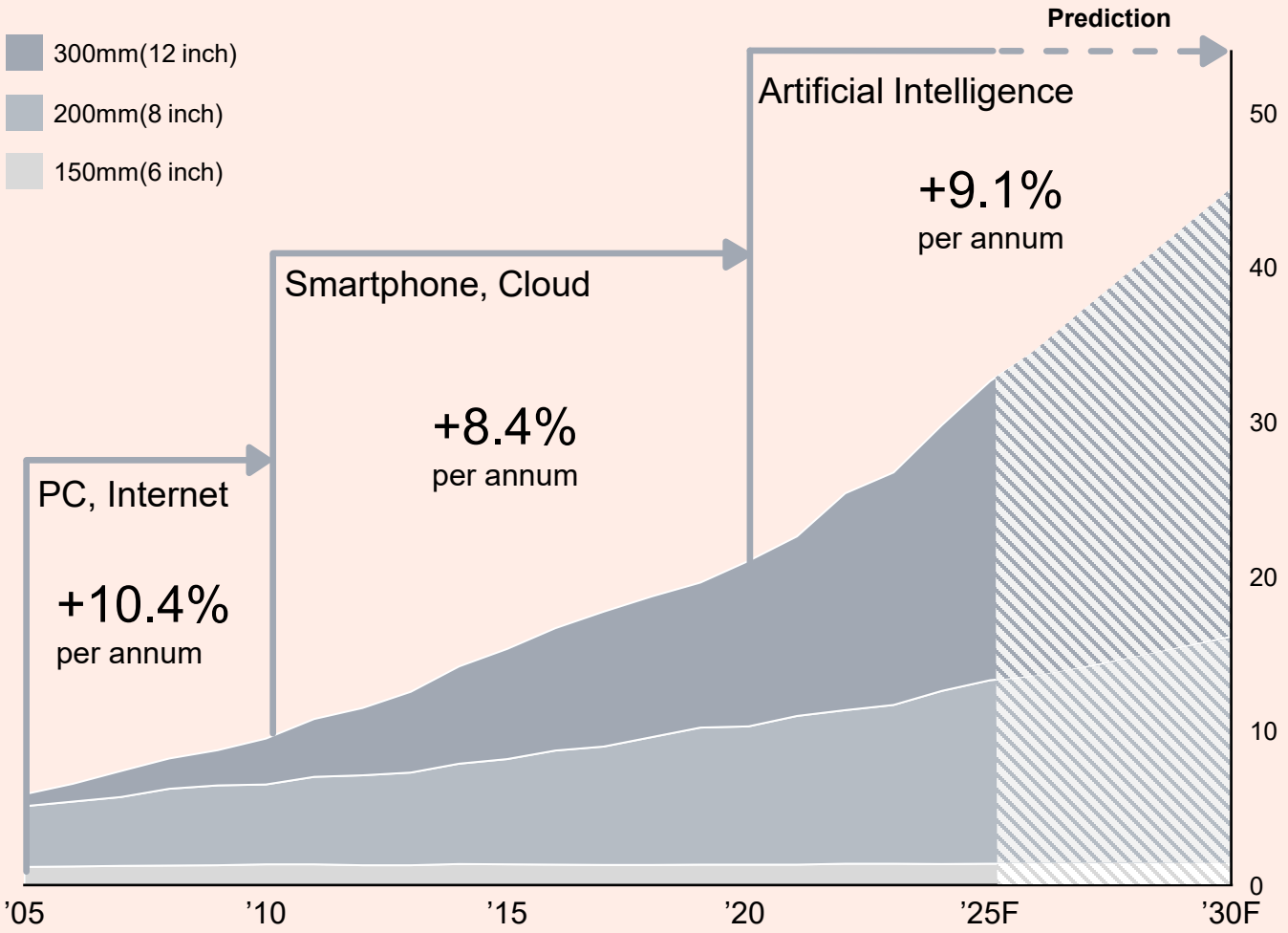
Significant differences in strategies by territory are evident among the Logic, Memory, and DAO (Discrete, Analog, Opto) sector. Some seek to maintain their position in areas where they have previously established strength, while others attempt to venture into new domains.

As global demand for high-performance, energy-efficient and highly reliable chips continues to rise, large, versatile fabs that can run several technology nodes in parallel will likely be essential for keeping production on pace and sustaining the industry's next wave of growth.



Global fabrication capacity by wafer size

(Unit: Million wafer in 200mm equivalents per month)



Source: Company announcements, Expert interview, PwC analysis

Wafer capacity keeps growing

1990s to Mid-2000s (150mm → 200mm)
As fabs moved from 150 mm to 200 mm, larger wafers boosted die output and cut cost per unit. PC demand in the early Internet era accelerated 200 mm adoption, yet many 150 mm lines survived by pivoting to power discrete, MEMS and RF components.

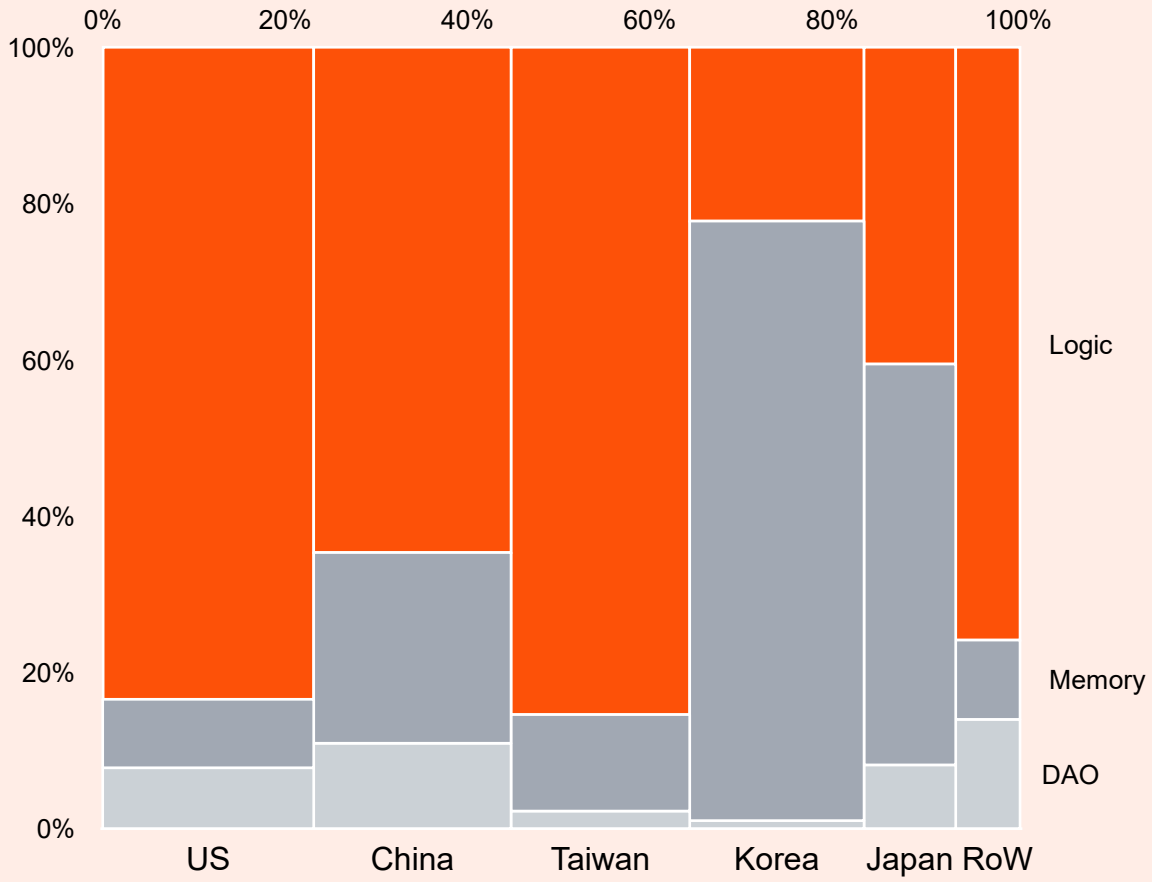
Late 2000s to 2010s (200mm → 300mm)
Intel, TSMC and Samsung brought 300 mm fabs into volume production as early as 2001, leveraging full automation and better economies of scale. Memory IDMs quickly followed, and foundries expanded 300 mm capacity for advanced nodes. After a brief lull, 200 mm saw a second wave of investment from 2016 onward—driven by IoT sensors, CMOS image sensors and power ICs—particularly in China and Southeast Asia.

2020s and beyond
With 450 mm development shelved on cost grounds, 300 mm remains the workhorse for advanced node logic and DRAM/3D NAND ramps. At the same time, demand for SiC, GaN, analog and specialty imaging keeps 200 mm and 150 mm fabs busy, pointing to modest but steady growth across all three wafer sizes through 2030.

Global semiconductor fab investments

(Unit: Million wafer in 200mm equivalents per month)

Sum of '24-'30F: **$1.5 trillion+**



Source: Company announcements, Expert interview, PwC analysis

Gold-Rush spending on new fabs

The United States and China hold title as leading spenders in the semiconductor industry. China pursues self-sufficiency to offset U.S. export controls, while the United States channels massive capital into new facilities to strengthen its domestic chip sector.

In the logic semiconductor segment, advancements in AI and high-tech fields have made logic chips critical, garnering the largest share of funding. The United States and Taiwan are expanding investments in advanced nodes, while China mainly focuses on relatively legacy nodes against restrictions on advanced equipment import.

Korea will likely sustain its memory market leadership with significant investments in DRAM and NAND flash, emphasizing scale and price competitiveness. As high-bandwidth Memory (HBM) emerges as essential for AI, Korean semiconductor leaders are increasing spending to bolster their position.

DAO semiconductors generally require less technological complexity than logic or memory, often leading to lower capital expenditure. China's prominent spending in DAO may be considered an attempt to mitigate restrictions on high-end equipment by concentrating on areas with relatively lower barriers to entry.

Fueled by strategic investments, global semiconductor fab spending from 2024 to 2030 is projected to exceed $1.5 trillion—equaling the total of the past two decades. As the AI boom accelerates, logic semiconductors are expected to further boost investment, potentially pushing fab spending even higher during this period.

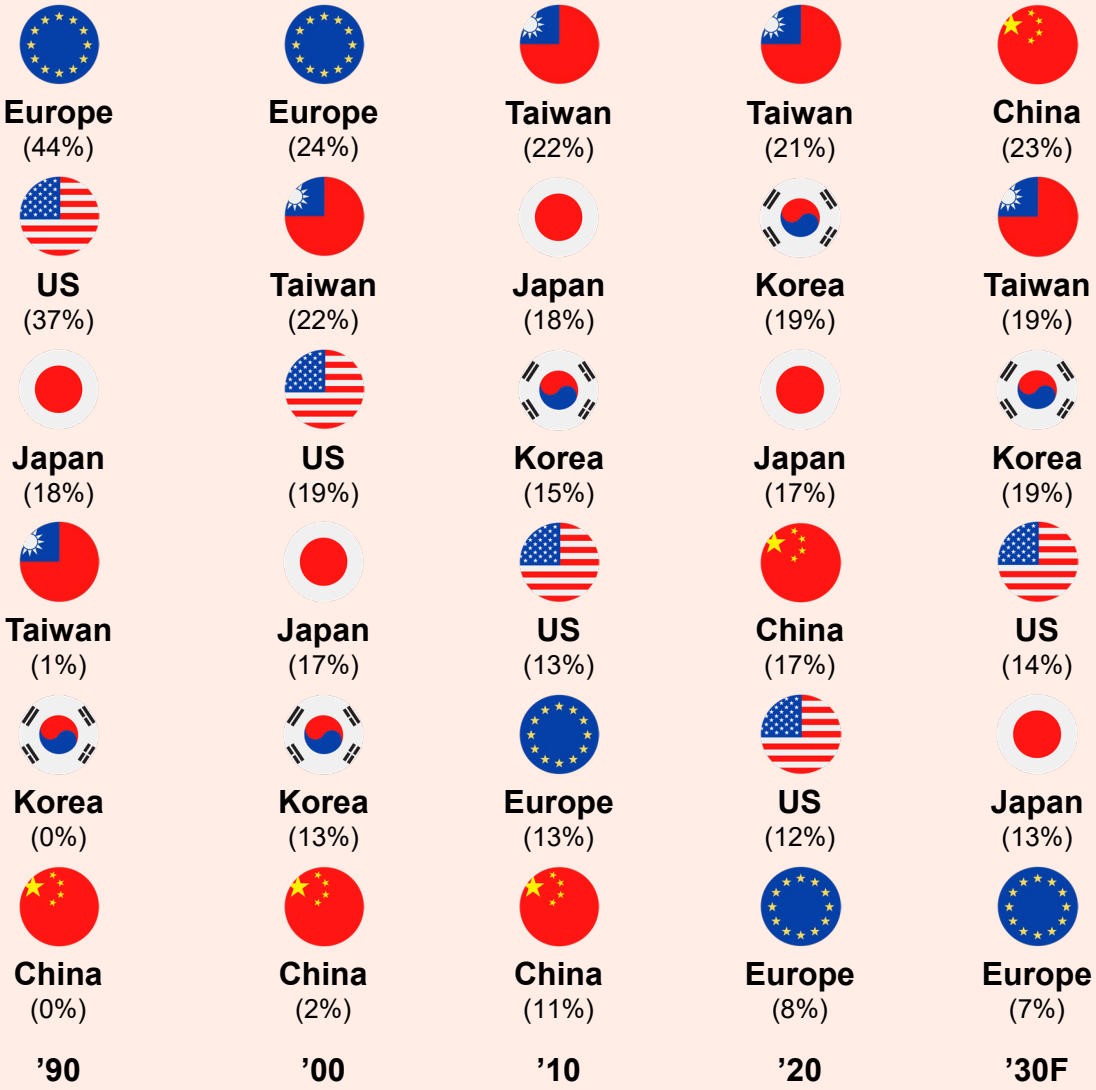
Semiconductors through time: Past, present, and future

Before 2000: The dawn of the industry
From the 1960s through the late 1990s the chip sector moved from laboratory curiosity to mass production. Pioneers such as IBM and Motorola in the United States, Philips and STMicroelectronics in Europe, and Toshiba, NEC, Hitachi and Samsung in Asia drove breakthroughs in memory, microprocessors and lithography. Commercial ICs first appeared in the mid 1960s but exploding demand for PCs and consumer electronics in the 1980s and 1990s set the stage for the industry's long-term expansion.

2000–2020: The growth era
During the early 2000s, increasing amounts of capital poured into advanced process technology. Korea greatly expanded domestic DRAM and NAND fabs, while Taiwan's TSMC perfected the pure-play foundry model; by the mid 2000s Taiwan led the world in outsourced logic capacity. A growing roster of U.S. and European companies adopted the fabless strategy, handing wafer production to Asian foundries and OSATs and further shifting the supply chain eastward.

2030 forecasting: A new chapter
China, backed by heavy state incentives, is pouring billions into mature node logic and memory; SMIC and YMTC are adding capacity—still a node or two behind the frontier—while dozens of local and foreign firms break ground on new fabs. The United States is countering with CHIPS Act subsidies to lure advanced logic and heterogeneous integration fabs. Korea and Taiwan aim to reinforce their respective dominance in memory (especially HBM) and transformative foundry services, while Japan and Europe roll out packages to attract both advanced logic and specialty SiC power lines. Collectively, these moves are set to realign global manufacturing by 2030 and usher in a new phase for the semiconductor industry.

Global wafer fabrication capacity share



Source: Company announcements, Expert interview, PwC analysis
* These figures represent major territories excluding the Rest of the World; the total may not add up to 100%

Capacity shifts to smaller nodes

A logic semiconductor — the “brain” that performs computation, control and signal processing — benefits from shrink in node size, because packing more transistors into the same area enables faster, more accurate operations.

Below 7 nm nodes offer top performance and power efficiency, fueling advanced AI accelerators and HPC solutions. With heavy foundry investments, their production share is rising. Sub-7 nm processes increasingly adopt industry leading transistor architectures and packaging for higher speed and power efficiency.

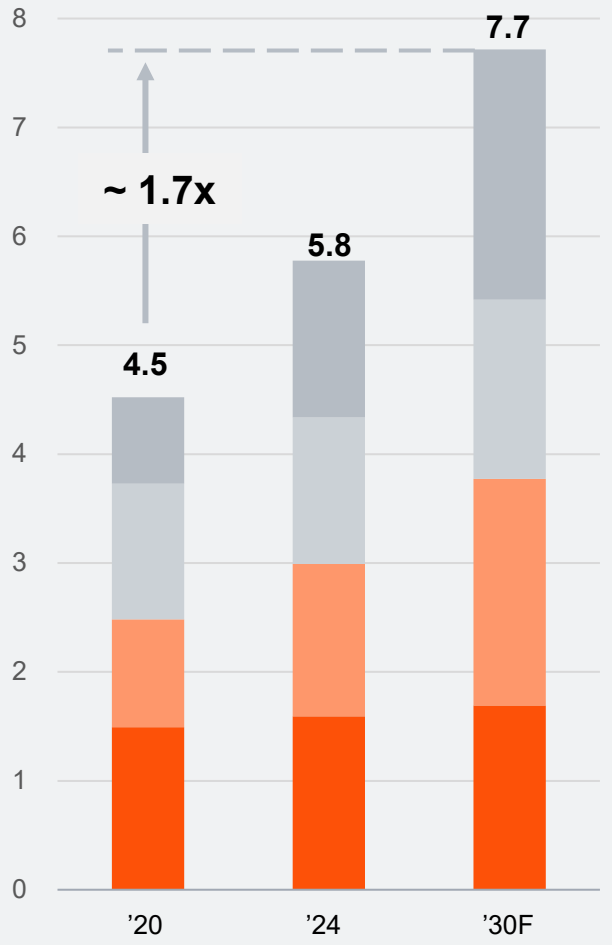
8–16 nm nodes occupy a middle range, delivering lower performance than sub-7 nm while being more costly than 22–28 nm. These nodes are commonly used in automotive ADAS, mobile SoCs, and mid-range graphics. However, their supply may see only a slight increase as nodes migrate directly from 22–28 nm to sub-7 nm for better performance.

22–28 nm nodes are often called “mature mainstream”. 22/28 nm lines underpin automotive MCUs, industrial IoT and consumer ASICs, where cost, voltage tolerance and proven reliability matter more than density. Demand is robust, but rapid 28 nm expansion in China could create local oversupply late in the decade.

32 nm and above serve price-sensitive or ultra-reliable devices — power controllers, sensors, display drivers, etc. Many suppliers operate in fully depreciated fabs, so profitability can persist even at lower volumes, but overall capacity will likely see a slight increase as nodes migrate to 28 nm and below for new designs.

Logic wafer fabrication capacity by node size[1)]

(Unit: Million wafer in 200mm equivalent per month)



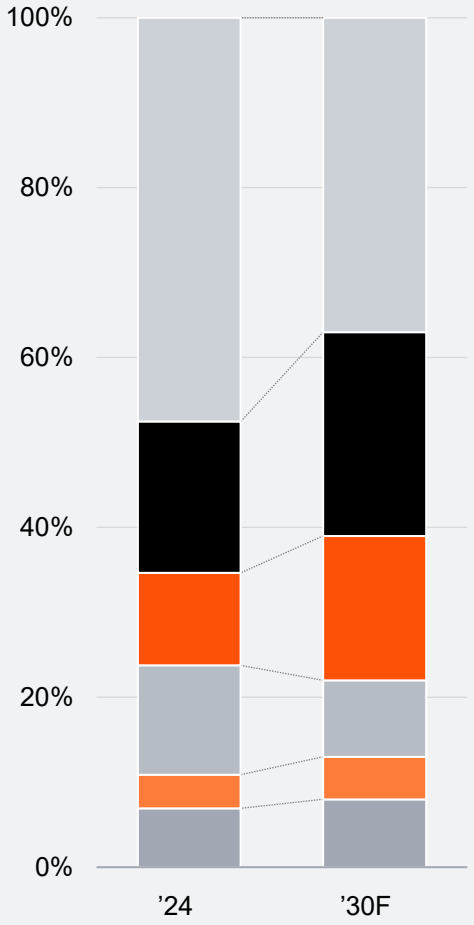
CAGR, 2024-30F

Total	+5%
≤ 7 nm	+8%
8 nm – 16 nm	+3%
22 nm – 28 nm	+7%
≥ 32 nm	+1%

1) Analysis conducted on 300mm wafer fabs only
Source: Company announcements, Expert interview, PwC analysis

Logic wafer fabrication capacity share[1)]

(Unit: Million wafer in 200mm equivalent per month)



Market share change

	'24	'30F	%Change
Taiwan	48%	37%	-11pp
China	18%	24%	+6pp
US	11%	17%	+6pp
Korea	13%	9%	-4pp
Japan	4%	5%	+1pp
RoW	7%	8%	+1pp

1) Analysis conducted on 300mm wafers only
Source: Company announcements, Expert interview, PwC analysis

Building resilience in logic chip

As semiconductors become strategic assets, governments are pouring incentives into advanced logic production. Pandemic-era shortages and geopolitical tensions have underscored how critical local capacity and stable supply chains are to national security.

In this evolving landscape, the U.S. is strategically leveraging the government support with subsidies, tax incentives, and infrastructure investments to attract advanced chip manufacturing. China, constrained by export controls, is substantially expanding capacity in mature logic nodes with strong state support. However, due to technology and equipment constraints, advanced nodes yields may remain relatively behind, meaning actual output may lag capacity.

Taiwan may maintain global leadership by focusing on advanced node production, though heavy investment in the most advanced processes keeps capacity expansion comparatively modest. Government support, including stable electricity, water supply, and an integrated chip ecosystem, may remain key to its sub-3 nm competitiveness.

Korea is likely to remain strong in memory manufacturing, yet it is strategically investing to increase its logic chip presence. Japan is revitalizing its chip sector through projects such as the TSMC–Sony Kumamoto fab, power device expansions and the Rapidus 2 nm fab, alongside a push for advanced packaging.

Taken together, these regional strategies are reshaping the geography of logic semiconductor supply, with resilience—rather than pure cost reduction—now the guiding principle for investment through 2030.

Next generation transistor architecture

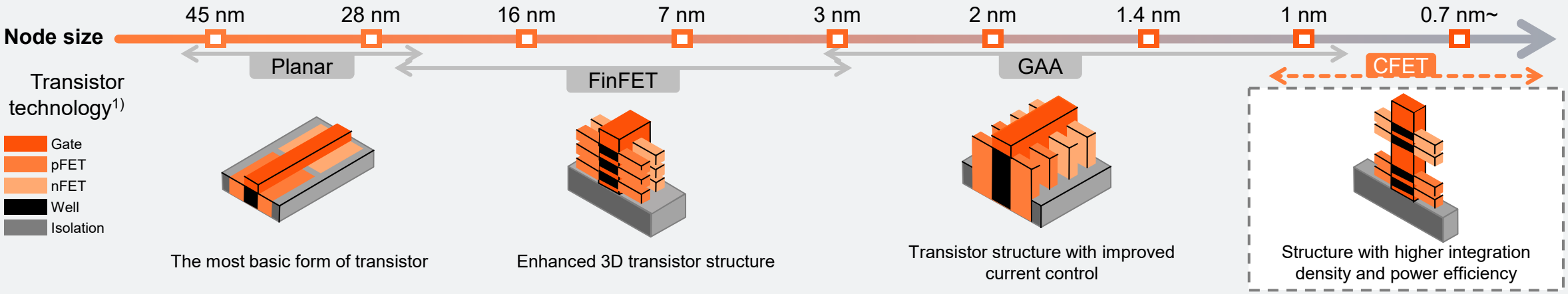
As chipmakers push below 5 nm, each process generation demands more R&D, capital and time. FinFET transistors reach their scalability limit around that point, so industry leaders are moving to gate-all-around (GAA) nanosheet devices at the 3 / 2 nm nodes. Shrinking farther can require fresh device architectures to curb short-channel effects, parasitic resistance and quantum tunnelling.

Two leading candidates are now on the table. Complementary FETs (CFETs) and Forksheet. CFET is a next-generation transistor architecture that enables higher integration density and performance. Intel, Samsung and TSMC are actively researching CFET, and while the commercialization timing varies by company, the market anticipates that initial commercialization could realistically occur in the early 2030s, if manufacturing and cost efficiencies significantly improve.

Between today's GAA and a full CFET stack lies the Forksheet concept, which introduces a dielectric "fork" to isolate adjacent nanosheet stacks and squeeze gate pitches even tighter. Some research consortia view Forksheet as a practical bridge, others may leapfrog it to focus resources directly on CFET.

Whichever path prevails, the post-2nm era can hinge on massive investment, new materials and advanced 3D integration—underscoring how fiercely the race for smaller nodes may continue to reshape the semiconductor landscape.

Timeline of major transistor technologies



1) Transistor technologies used at each node size can differ from one company to another

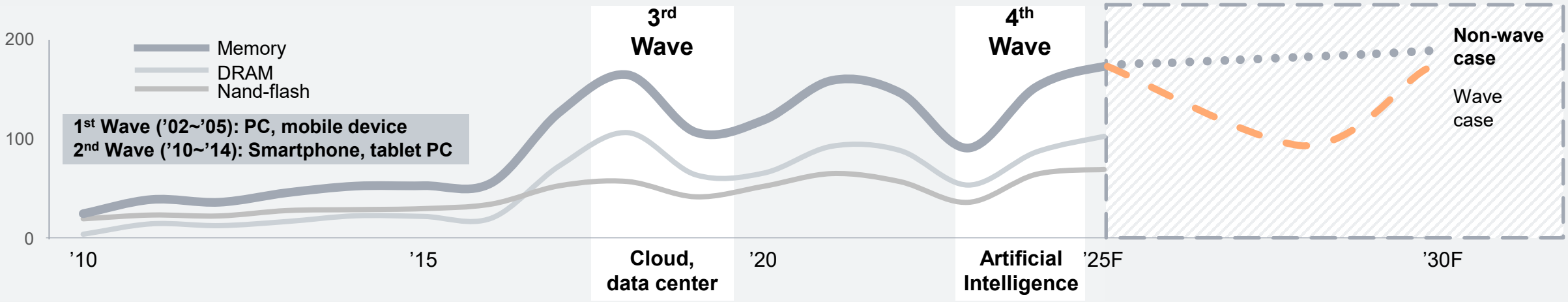
Is the memory super-cycle here to stay?

The memory market is famous for boom-and-bust "super-cycles." A wave typically starts when a new platform—smartphones, cloud servers, AI accelerators—soaks up capacity, sending prices and margins soaring. Usually, suppliers over-build, inventories swell and a down-cycle follows. Firms now temper that volatility with sharper production cuts, capital expenditure discipline and die-shrink pacing, but the pattern has yet to disappear.

Whether future cycles will moderate or not is up for debate. One camp believes tighter supply chain analytics, shorter equipment lead-times and HBM-style node diversification could smooth price swings. The other points to explosive AI workloads, autonomous vehicle data capture and edge computing growth as fresh demand shocks that may spark the next upturn. Emerging use cases such as mixed-reality headsets and smart industry sensors also underline memory's central role.

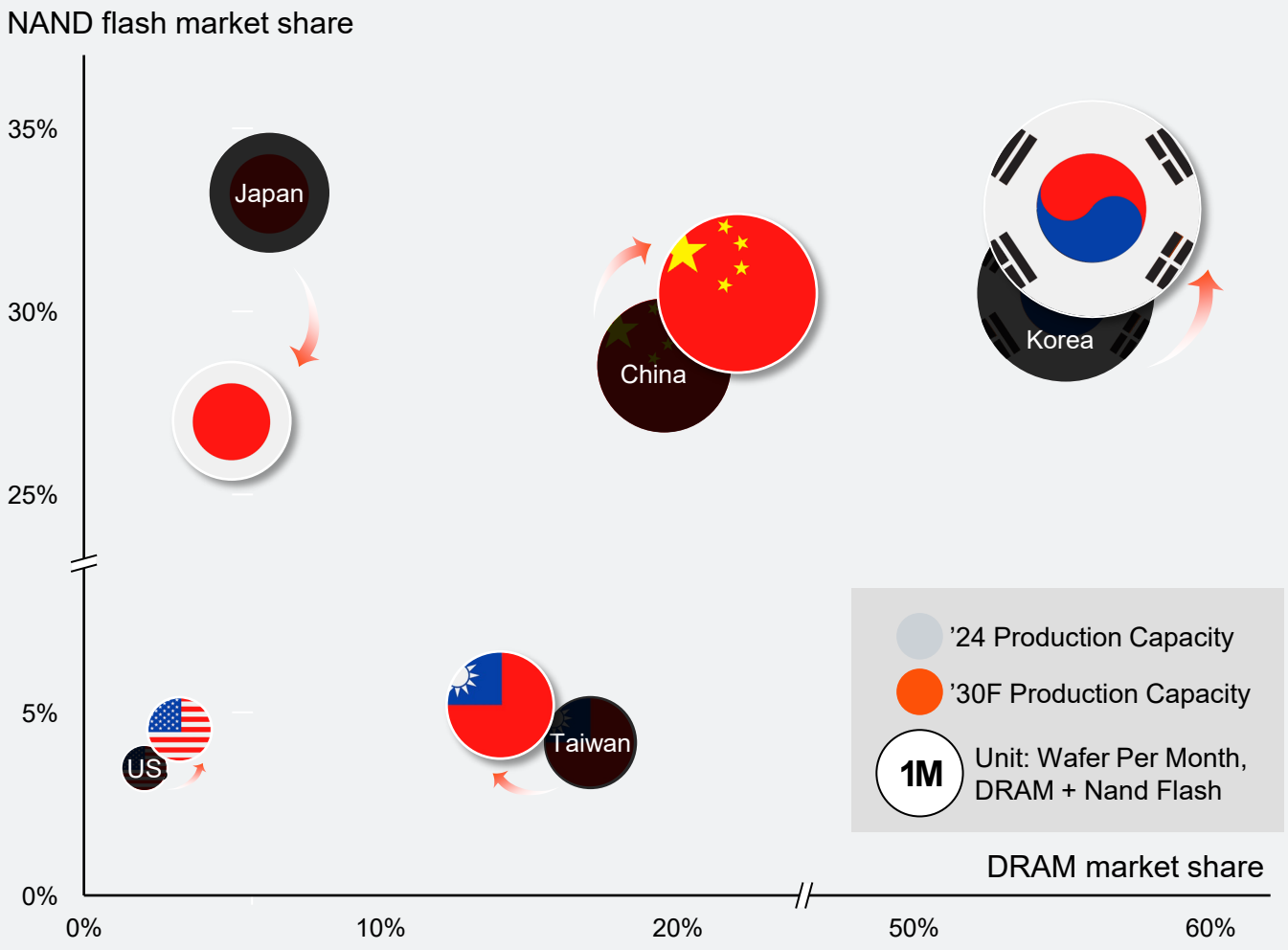
In practice, the depth of each cycle may hinge on three variables: the speed at which breakthrough applications ramp, the scale of manufacturers' capacity bets and the pace of process migrations that boost bits per wafer. Tracking those indicators—and adjusting investment accordingly—will likely be critical to navigating whatever wave comes next.

Global memory semiconductor market (Unit: $ Billion)



Source: Gartner, Expert Interview, PwC analysis

Memory wafer fabrication capacity share[1)]



1) Market share analysis based on the country/region of origin of memory fabrication facilities
Source: Company announcements, Expert interview, PwC analysis

Asia leads global memory shifts

Overall, the memory supply chain will likely stay Asia-centric, yet a broader regional balance is emerging.

Korea may maintain the strongest position in memory semiconductors, backed by advanced DRAM and NAND technologies and ongoing large-scale investments. Leveraging its established status, reliability, and quality, it is expected to preserve or even expand its presence.

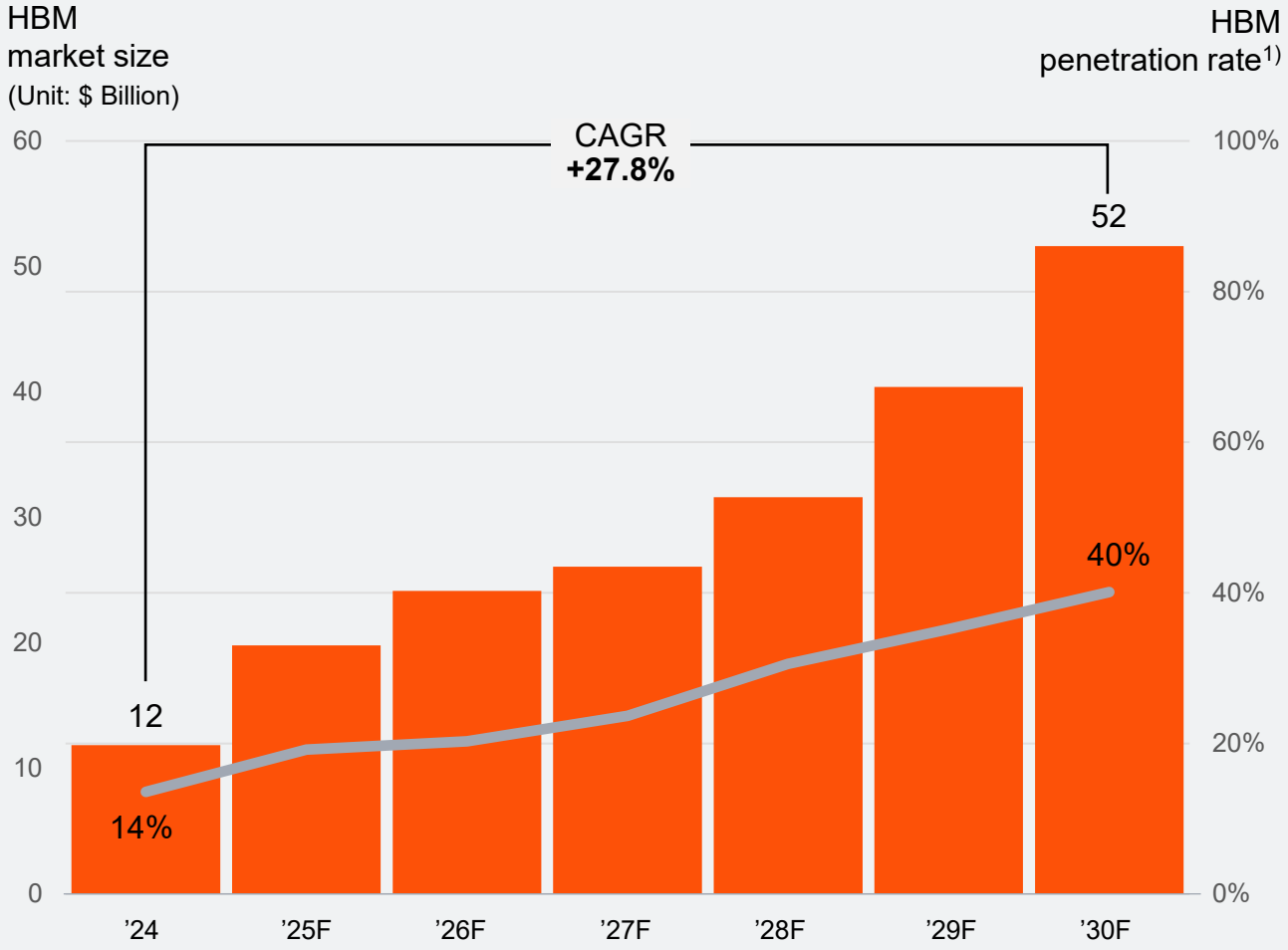
China is racing for self-sufficiency, building dozens of mature node memory lines under generous state subsidies. Domestic suppliers are improving yields in mainstream DRAM nodes and ramping high-layer 3D NAND.

Japan, once strong in NAND flash, may see its share slightly decline by 2030 due to weaker cost competitiveness. Also, Its focus on gaming and telecommunications, not projected for robust growth, may further limits expansion.

Taiwan may focus on cost-efficient mid-range DRAM and specialty NOR/SRAM lines. Lacking large-scale NAND capacity, the island's share of the NAND market is relatively unlikely to grow meaningfully.

United States is using government incentives to establish domestic memory manufacturing. New DRAM and 3D NAND mega-fabs are under way. These plants may nudge U.S. share upward toward the end of the decade.

HBM market size and penetration rate over DRAM



1) Penetration rate: The proportion of HBM within total DRAM
Source: Omdia, PwC analysis

AI boosts HBM demand

The surge of generative-AI training and inference has turned high-bandwidth memory (HBM) into a critical component of modern data center servers. CPU, GPU and accelerator performance keeps climbing, but if the attached memory cannot supply data fast enough the entire workload can experience bottleneck.

HBM tackles that bottleneck by stacking multiple DRAM dies on a tiny base-logic die, connecting them with through-silicon vias (TSVs) and mounting the stack on a silicon interposer right next to the compute chip. This 3D integration delivers terabytes-per-second bandwidth in a very small footprint, making HBM crucial for power-hungry AI and HPC systems.

Many suppliers are rushing to add capacity, yet shortages can still appear. First, demand may outrun even the most optimistic forecasts, and the 18-to-24-month lead time for new TSV lines leaves little room for quick fixes. Second, the supply chain is only as strong as its weakest link: limited availability of silicon interposers, advanced bumping capacity, or the specialized base-logic die can all throttle overall HBM output.

Until packaging infrastructure scales in parallel with DRAM wafer starts, tight HBM supply—and premium pricing—are likely to persist.

Bigger wafers, broader supply: DAO's transition

Discrete semiconductors

Most power MOSFETs, IGBTs and diodes still run on 150–200 mm wafers, but a rising share is shifting to 300 mm—led by high-value devices like low-voltage MOSFETs, automotive IGBTs and Smart-Power ICs. Meanwhile, SiC and GaN parts are scaling on 200 mm and pilot 300 mm tools, foreshadowing a wider 12-inch move later this decade.

Analog semiconductors

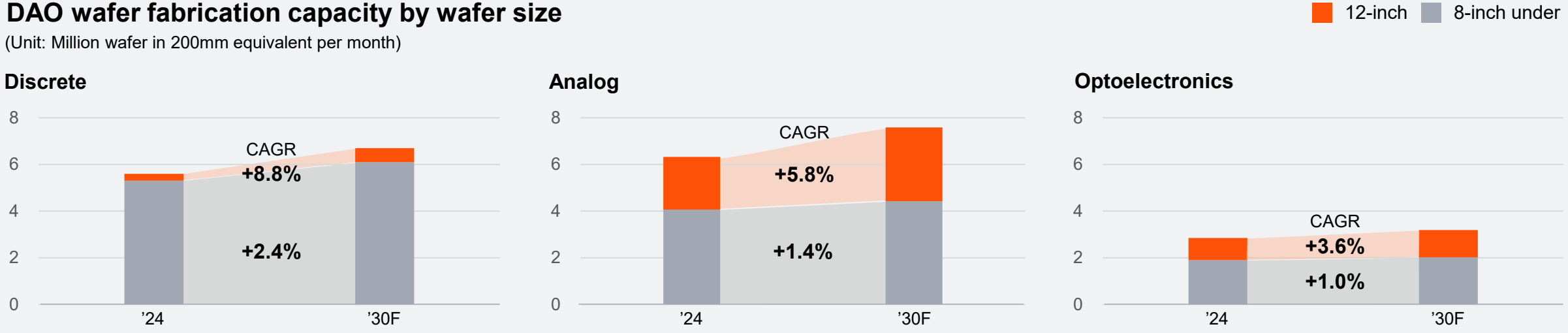
PMICs, amplifiers and RF front-ends long lived on 200 mm tools, but rising die area and tighter process tolerances are pushing wafers toward 300 mm. The lock-in nature of analog design generally keeps revenue stable, yet migration requires careful yield learning, so most suppliers can pursue a phased roadmap from 200 mm to 300 mm.

Optoelectronic semiconductors

LEDs and most laser devices are still made on 100 – 150 mm compound semiconductor or sapphire wafers, whereas CMOS image sensors have largely shifted to 300 mm lines to boost pixel density. Moving these compound semiconductor processes to larger wafers is possible but slower, because the specialized equipment and process steps typically need to be re-qualified first.

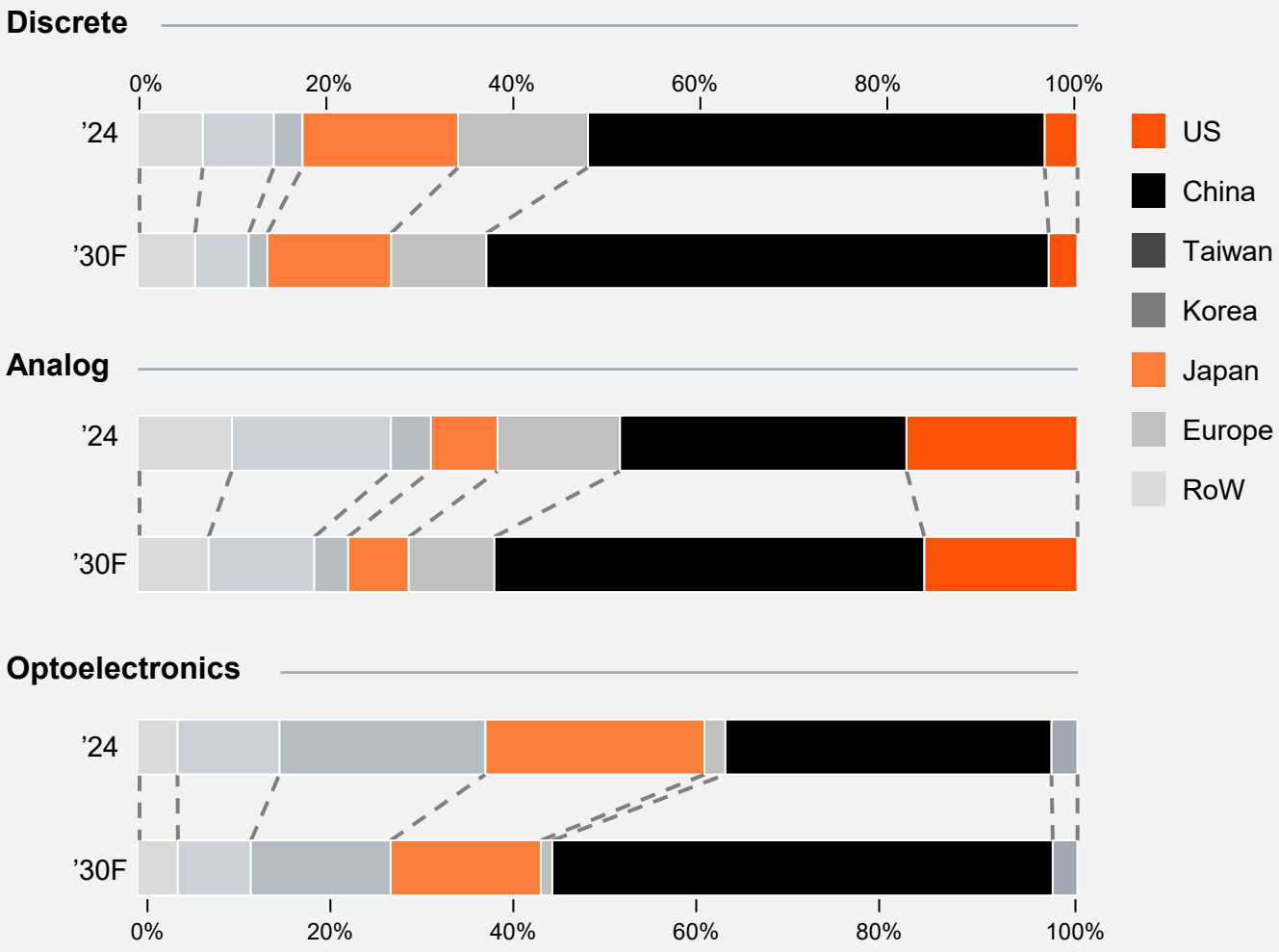
DAO wafer fabrication capacity by wafer size

(Unit: Million wafer in 200mm equivalent per month)



Source: SEMI, Expert Interview, PwC analysis

DAO wafer fabrication capacity share



Source: Company announcements, Expert interview, PwC analysis

Slow but steady growth

Because DAO devices rarely require the most advanced tools, capital intensity is relatively lower than for advanced node logic and memory. Large, one-off mega-fab announcements are uncommon, yet many regions continue to add DAO capacity incrementally to enable baseline domestic supply.

China is expanding the fastest on the back of strong local demand for power, analog and optoelectronic chips in energy, telecom and industrial equipment. Numerous mid-tier suppliers are using cost advantages to capture price-sensitive segments.

United States incentives are funding new analog and mixed-signal fabs that serve high-value aerospace, defense and industrial markets, aiming to rebuild domestic capability without chasing commodity volumes.

Japan may maintain a firm position in discrete power devices and sensors for its automotive and precision-equipment sectors. Although mature-market saturation may slow growth, the shift to electric vehicles is likely to sustain demand for Japanese SiC power components.

Overall, DAO capacity may increase slowly but steadily worldwide, reinforcing supply chain resilience without the large-scale attention drawn by advanced logic or memory projects.

The evolution of power semiconductor

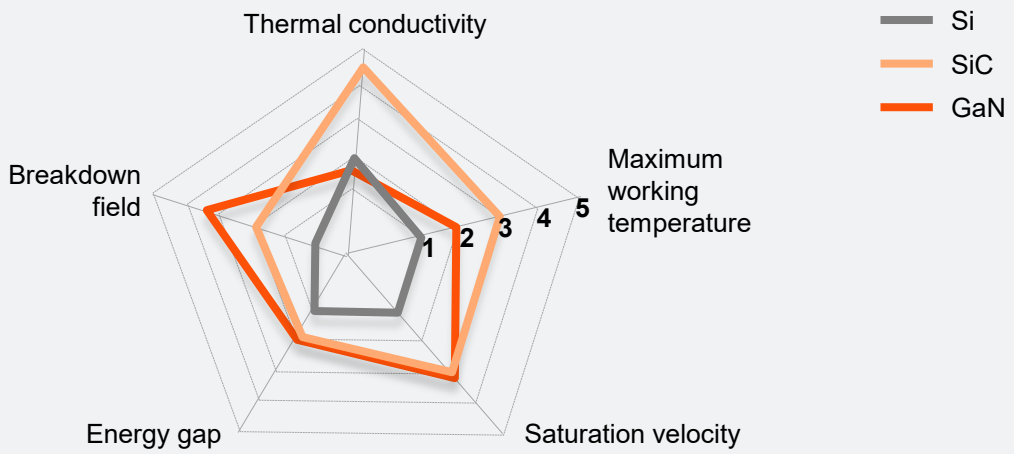
Silicon (Si) has long been used in power electronics due to its affordability and established production processes. However, wide-bandgap (WBG) semiconductor materials, particularly silicon carbide (SiC) and gallium nitride (GaN), are gaining popularity because they operate at higher temperatures, higher voltages, and offer faster switching speeds than silicon.

SiC is highly effective in high-voltage and high-current applications, making it ideal for electric vehicle (EV) traction inverters, renewable energy converters, and heavy industrial drives. Manufacturers are transitioning from 150-mm to 200-mm SiC wafers to lower costs and enhance wafer quality.

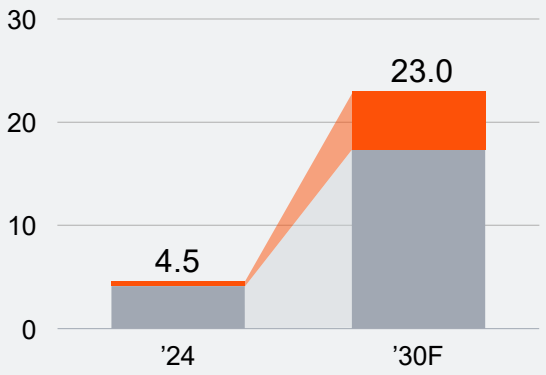
GaN excels in products requiring rapid switching and compact size, such as USB-C fast chargers, laptop adapters, 5G base station power supplies, and high-frequency converters for data centers. Its structure also enables easy integration with standard CMOS control chips, simplifying device design.

Despite the production of hundreds of millions of WBG devices, supply limitations persist due to costly and time-intensive processes like crystal boule growth, wafer polishing, and advanced epitaxy. Short-term shortages remain possible, especially for 200-mm SiC substrates and high-voltage GaN wafers. However, continued investment in larger wafers, improved yields, and advanced equipment will gradually alleviate these constraints, narrowing the cost gap with silicon and speeding up adoption of SiC and GaN solutions.

Power semiconductor : Performance comparison



Power semiconductor market by material (Unit: $ Billion)



CAGR, 2024-30F

Total	+30.9%
GaN	+53.5%
SiC	+27.0%

Source: Omdia, PwC analysis

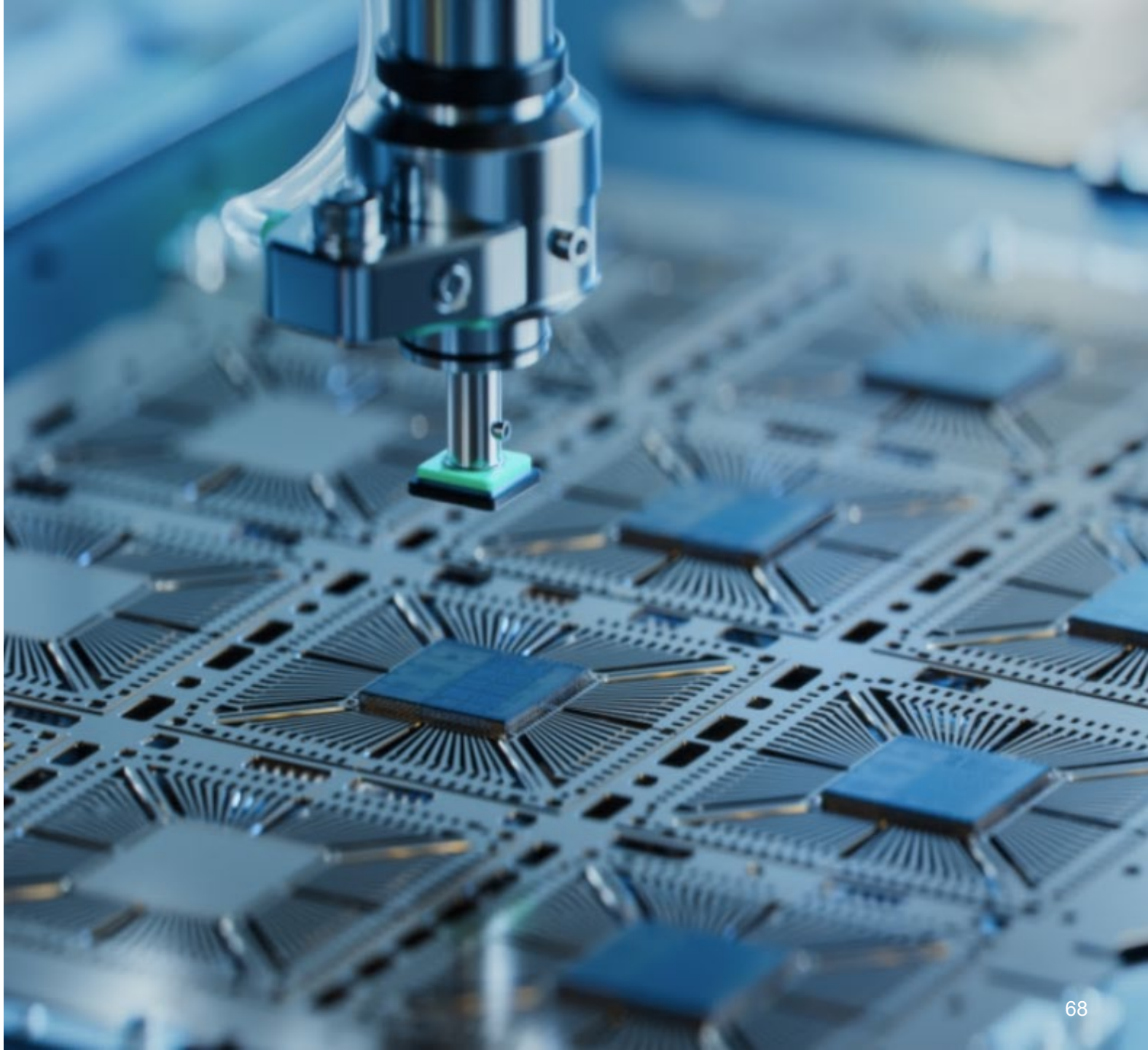
Packaging and Testing

Packaging and test no longer simply protect finished dies; they now enhance die-to-die connectivity and improve electrical and thermal reliability under harsh conditions.

As transistor scaling delivers diminishing returns, advanced packaging has become a prime lever for system performance. Key innovations include shorter, high-bandwidth interconnects and chiplet architectures that assemble heterogeneous dies in a cost-effective, flexible manner.

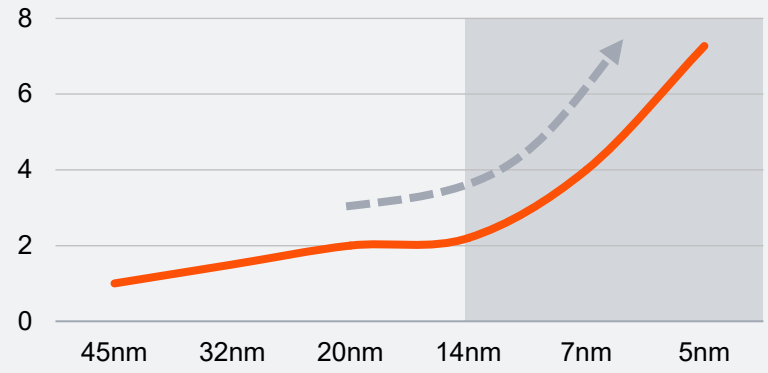
Rising assembly complexity makes defect prevention and yield improvement critical, spurring rapid progress in optical, X-ray and system-level inspection tools.

Looking ahead, meaningful performance gains may depend on the tight co-evolution of front-end transistor technology and back-end packaging and test processes.



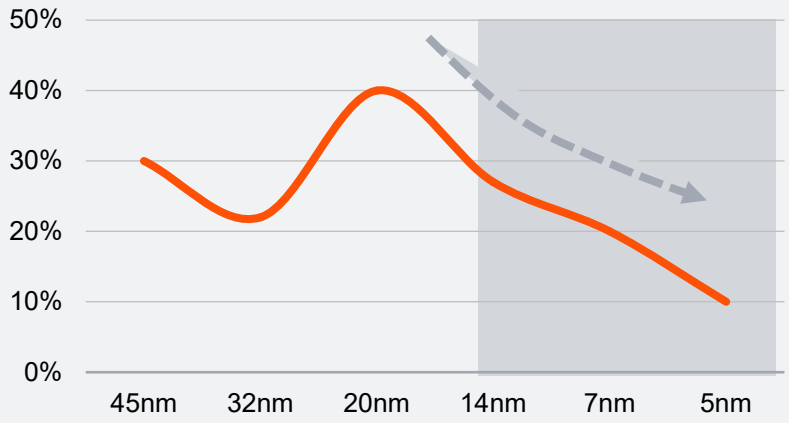
Front-end costs keep rising…

Wafer manufacturing cost by node (45 nm=1)



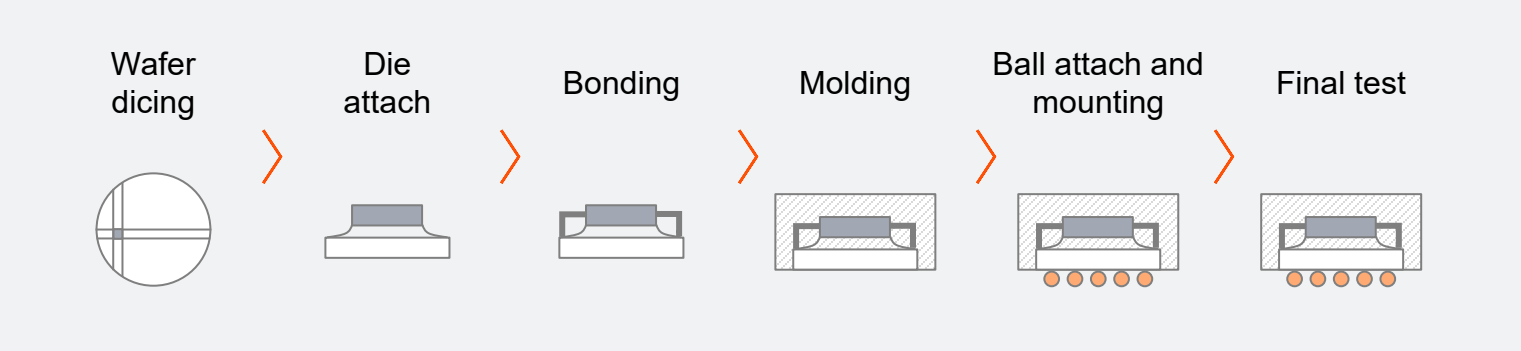
…While its benefits are questionable

Performance improvement by node



Source: AMD, PwC Analysis

Back-end pushes the limits further



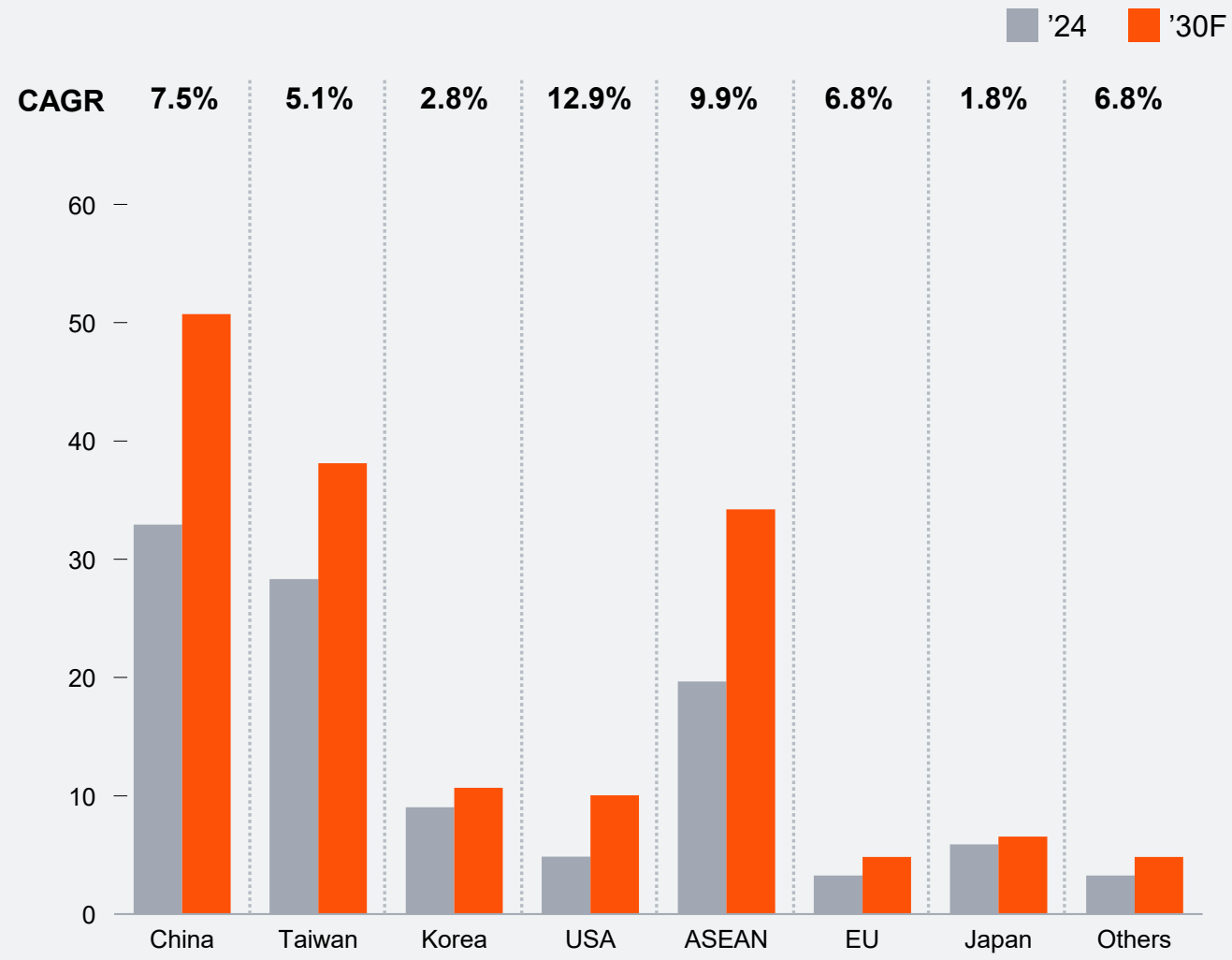
For decades, performance gains came primarily from front-end miniaturization, but once process technology pushed below 10 nm only two foundries could manufacture such nodes in volume, with a third now ramping. At these dimensions, short-channel effects, parasitic capacitance and rising leakage currents make each shrink far harder and costlier.

Early CMOS shrinks—90 nm to 28 nm—often doubled transistor density and improved power-performance by 25–50 %. From 16 nm FinFET down to today's 3 nm nodes, the density curve has flattened, and efficiency gains have slowed, while wafer cost has nearly tripled and die-level economics have risen by roughly two- to three-fold. EUV lithography tools, lower initial yields and soaring R&D budgets underline how expensive additional front-end scaling has become.

Faced with these diminishing returns, chipmakers are putting renewed emphasis on advanced back-end techniques—chiplets, 2.5D interposers and 3D stacking—to keep system-level performance moving forward even as front-end progress decelerates.

Global semiconductor packaging and testing market

(Unit: $ Billion)



Source: Company announcements, Expert interview, PwC analysis

Betting on back-end processes

China – State funds are pouring into new wafer-level packaging plants, while local OSATs upgrade for chiplet assembly and high-speed AI interconnects.

Taiwan – Foundries and OSAT leaders are scaling 2.5D/3D capacity and building campuses for signal-integrity and system-level test, pairing advanced back-end with advanced front-end nodes.

Korea – A national cluster focused on 3D stacking, chiplets and reliability test is under way, backed by shared R&D tools and workforce training.

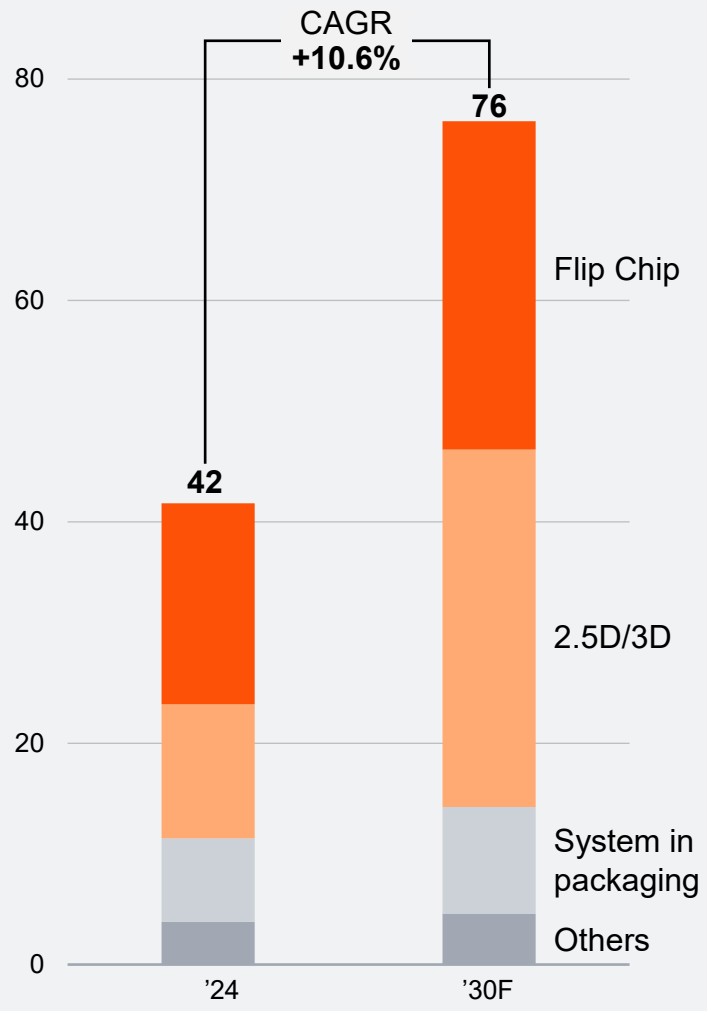
United States – Federal incentives support a network of packaging R&D hubs and pilot lines to advance chiplet standards, thermal solutions and fast reliability screening.

ASEAN – Malaysia strengthens its OSAT base to attract advanced packaging projects, while Vietnam targets back-end investment as its gateway into semiconductors.

Together these moves show that advanced packaging and test are becoming as strategic as front-end scaling in the next wave of chip competition.

Global advanced packaging market

(Unit: $ Billion)



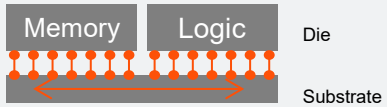
Source: Yole Group, PwC analysis

Shorter interconnects and greater efficiency

In advanced packaging, precision and cleanliness have become as crucial as they are for front-end fabs, prompting a steady increase in investments by foundries and IDMs.

Flip-chip packaging

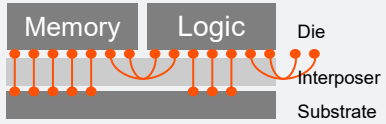
Inverts the die for direct substrate connection



- Uses bumps instead of traditional wire bonding
- Shortens signal paths, reducing latency
- Widely used in ASICs

2.5D packaging

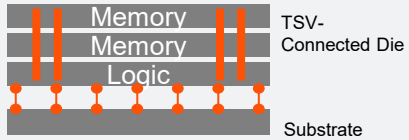
Multiple dies are placed horizontally on interposer



- Allows in-package communications, reducing signal path lengths
- Widely used in data centers, and advanced computing

3D packaging

Dies stacked vertically for higher integration

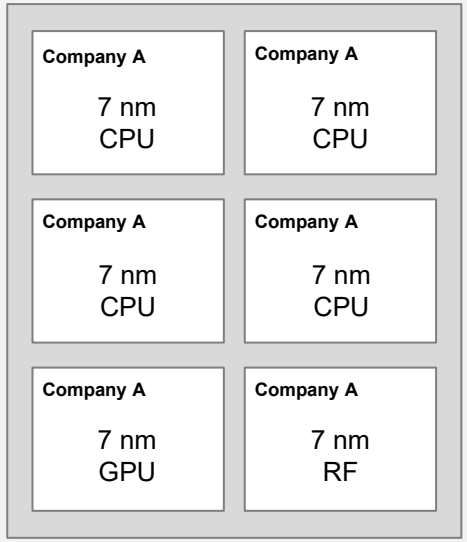
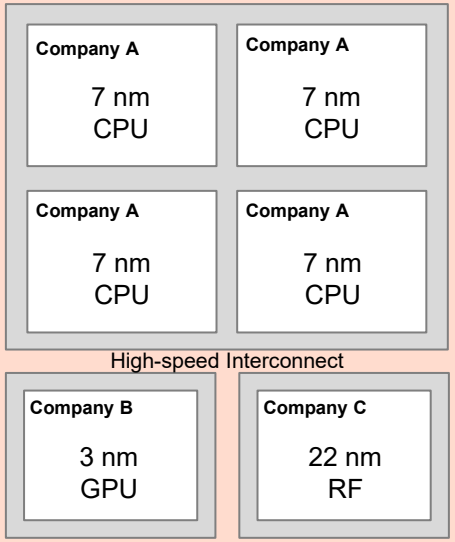


- Through-Silicon Vias (TSVs) for direct chip-to-chip contact.
- Reduces interconnect length, achieving higher speed.

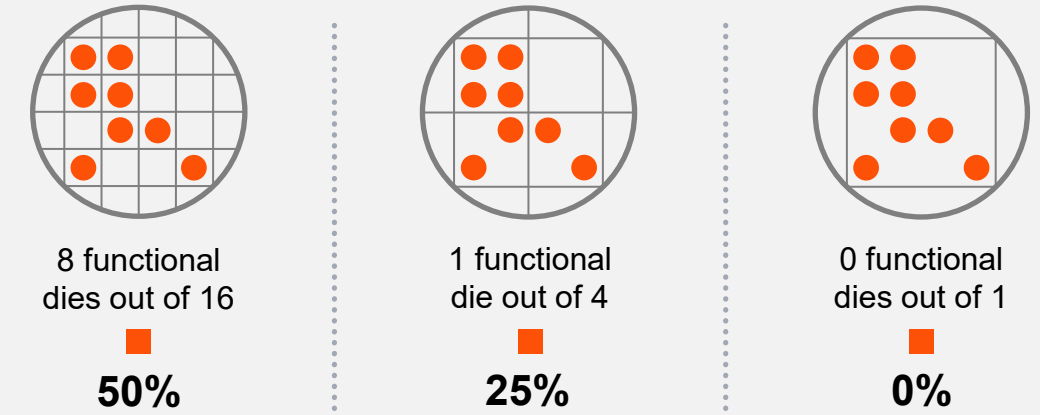
IDM and foundry take lead in packaging innovation

Advanced packaging is now a main engine of chip performance, yet its 3D and chiplet flows demand fab-class precision. As a result, foundries and IDMs control about two-thirds of advanced packaging investments and will likely keep driving the biggest breakthroughs. OSATs, meanwhile, are stretching into fan-out and 2.5D packaging to handle overflow volume and mid-range designs, enabling the back-end ecosystem keeps pace with growing demand.

Efficiency through flexible heterogeneous integration

	Monolithic die	Chiplet
Definition	Manufactures a processor as a single, large silicon die, offering high performance, lower latency	Multiple smaller dies within a package, improving scalability, cost efficiency, and yield
Concept		

Effect of die size on yield

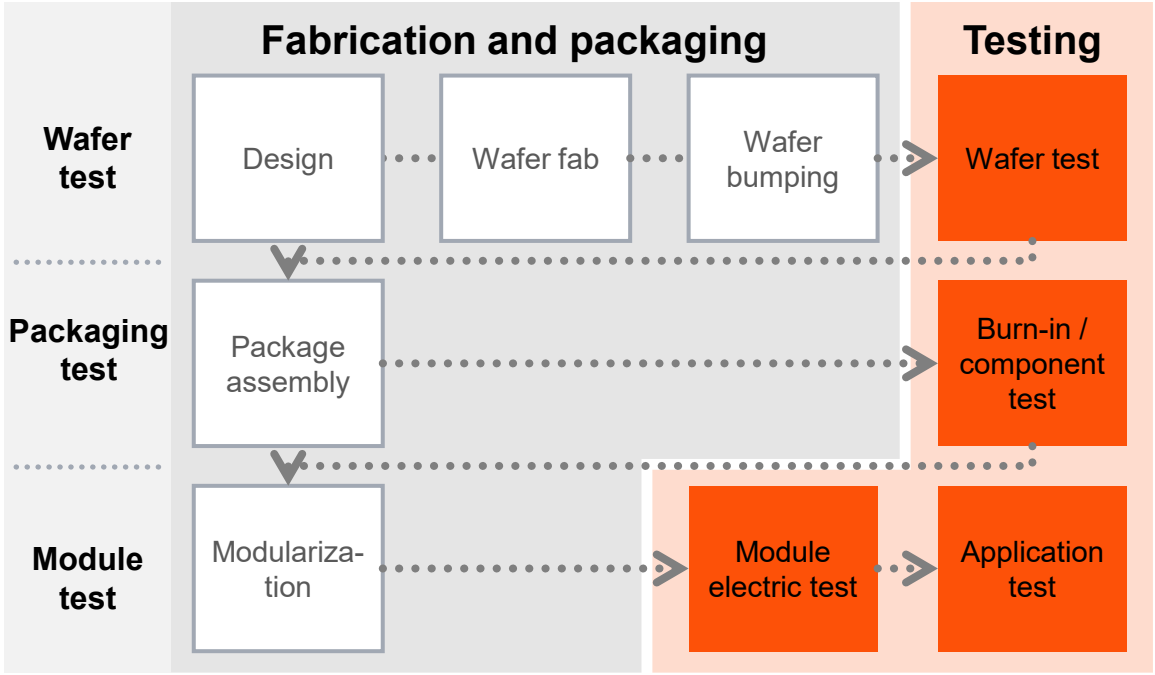


Faster development

Chiplets enable selective upgrades without redesigning the entire chip. A CPU die may stay on 16 nm while an AI tile jumps to 5 nm, cutting redesign effort and time-to-market.

Strategic specialization

Firms can keep core IP in-house and source other chiplets externally. As adoption grows, multi-foundry builds, open interconnect standards and advanced packaging skills become critical, making design houses experienced in cross-foundry collaboration increasingly valuable.



Wafer testing — Key to higher yield

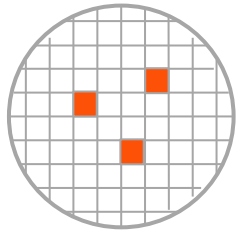
As the industry shifts from monolithic die architectures to heterogeneous integration and advanced multi-die packaging, including 2.5D and 3D architectures, the importance of wafer level testing has grown significantly. With high-yield, miniaturized dies becoming the norm, assessing individual die quality before assembly is crucial to enhancing overall yield. A single defective die can compromise an entire package, making rigorous wafer screening essential to reducing yield loss and enabling functional integrity. On the packaging test front, the scope has expanded beyond traditional electrical inspections. As stacking technologies advance, thermal durability tests, burn-in testing, and high-resolution non-destructive evaluations like X-ray and CT scans are increasingly used to detect latent defects and enhance reliability.

The landscape of semiconductor testing

Among semiconductor testing stages, wafer testing has the highest correlation with yield enhancement. Unlike packaging test, which occurs later in the process, wafer testing screens defects at the die level, preventing faulty components from advancing. In multi-die packages, even a single defective die can render the entire package unusable, making early defect detection critical.

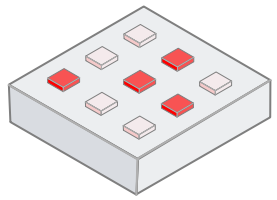
As wafers become thinner, contact-based testing faces limitations, leading to the adoption of non-contact optical inspection (e.g., OCT, IR). Additionally, as process nodes shrink, Probe Cards are also miniaturizing to enable precise electrical testing, further enhancing yield and efficiency.

Wafer sort test



Wafer pre-dicing stage

Known-good-die test



Individual dies after singulation

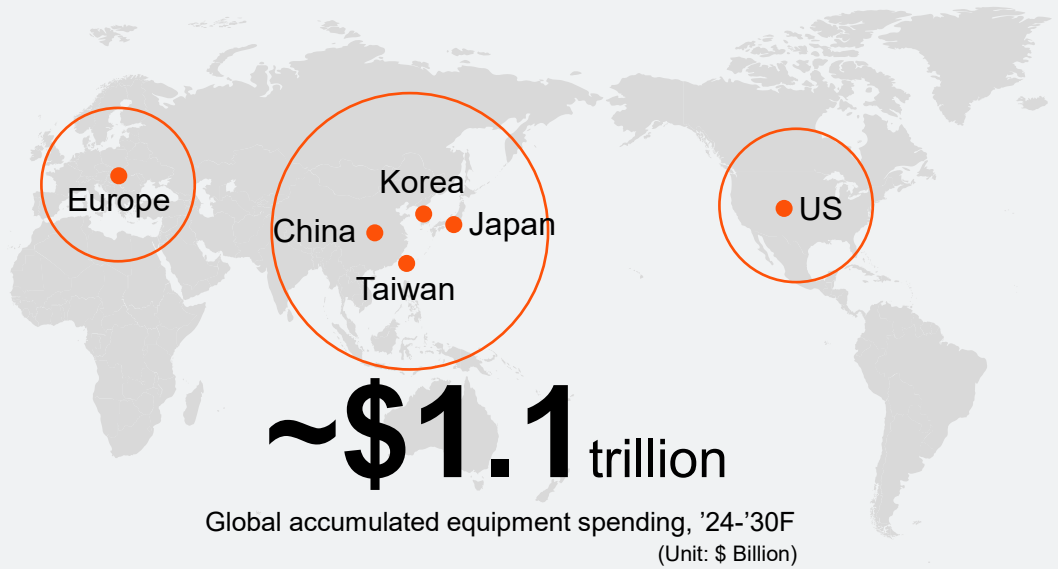
Equipment and Material

As process technology advances, both front-end fabs and their tool suppliers are running into steeper technical barriers. EUV lithography, now required for 7 nm nodes and below, hinges on extreme-precision lasers and optics, and its availability remains constrained because a single company supplies the EUV equipment.

On the back-end, hybrid bonding for next generation 3D packaging poses its own hurdles. Only a few tool vendors make qualified wafer- and die-level bonders, but additional entrants are expected to relieve this constraint sooner than the front-end EUV bottleneck.

With capital intensity rising across the board, access to specialized equipment and materials is now a critical requirement for adding new wafer capacity, intensifying global competition among manufacturers and tool makers alike.

Accumulated semiconductor equipment spending



~$1.1 trillion

Global accumulated equipment spending, '24-'30F

(Unit: $ Billion)

EMEA	6%	APAC	69%	NA	23%
Europe	62	Japan	96	US	240
		Korea	211		
		China	219		
		Taiwan	220		

Rest of World : $21 Billion (2%)

Source: Company announcements, Expert interview, PwC analysis

Asia continues to fuel semiconductor equipment spending

Global semiconductor equipment spendings are expected to grow at an annual rate of 7.4% until 2030, with over 70% of these investments concentrated in Asia. While Asia's share peaked at around 80% in the early 2020s, the 2022 CHIPS Act increased U.S. capital expenditure, slightly reducing Asia's share. Nevertheless, Asia continues to dominate due to its robust manufacturing ecosystems and efficiency. The lower share of Western regions is also attributed to their focus on fabless operations, while Asia specializes in semiconductor manufacturing.

Taiwan and Korea drive investments in advanced process technologies, focusing on sub-7 nm nodes. Samsung Electronics and TSMC are primary customers for ASML's EUV systems, which are essential for producing these nodes due to their extreme precision and feature scaling required for such advanced processes.

China is likely to account for a large share of Asia's semiconductor equipment purchases, yet most new capacity targets 28 nm and other mature nodes. Export controls from the United States, Japan, and the Netherlands restrict access to transformative tools. In response, domestic fabs are boosting high-volume production for automotive, IoT, and other markets while accelerating in-house R&D to reduce long-term dependence on foreign equipment.

Demand and supply of EUV

EUV lithography, first deployed for advanced node logic, has already moved into 1α-class DRAM and is spreading to successive memory nodes. Beyond the long-standing leaders in Taiwan and Korea, more demand is likely to come from U.S. and Chinese chipmakers, and Japan's Rapidus plans to enter 2 nm production later this decade—intensifying competition for a limited tool supply.

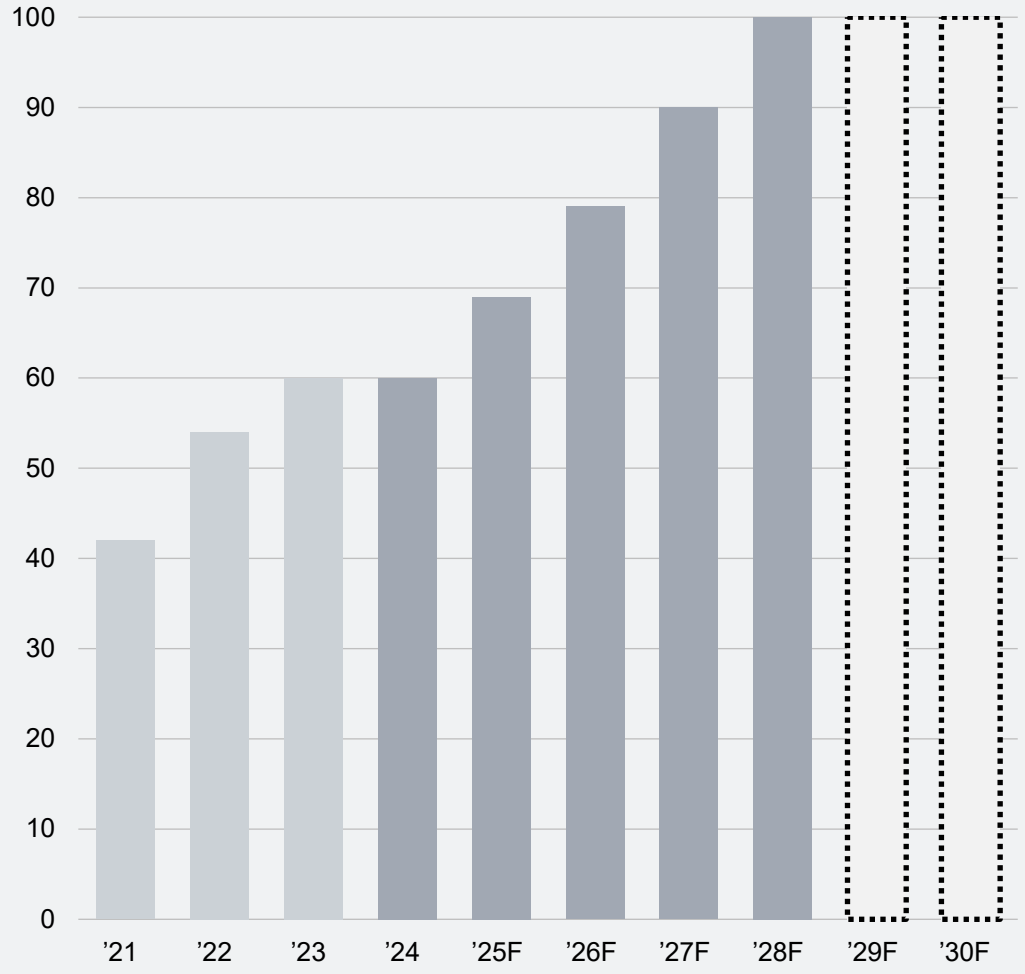
ASML is currently the only commercial EUV scanner vendor, shipping systems to major foundries and IDMs. The technology's extreme optics, vacuum and power requirements create formidable entry barriers. Alternative efforts exist—Canon is field-testing nano-imprint lithography for niche uses, and China's SMEE is filing EUV-related patents—but volume replacement for ASML's platform appears unlikely before 2030.

Even with ASML's capacity ramp, constraints persist. Each EUV scanner takes about twelve months to build and qualify, and the company's announced throughput through 2025 may not fully clear today's backlog. A key choke-point is the limited output of ultra-precise mirrors and other optics from Carl Zeiss SMT, which must stay contamination-free throughout the scanner's life.

Until new suppliers emerge, or radically different patterning methods mature, EUV availability will likely remain tight—and securing enough tools may be a central competitive factor for advanced node roadmap.

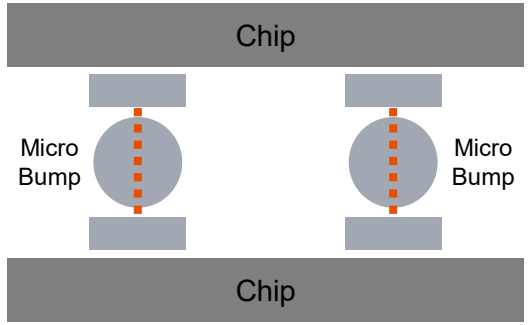
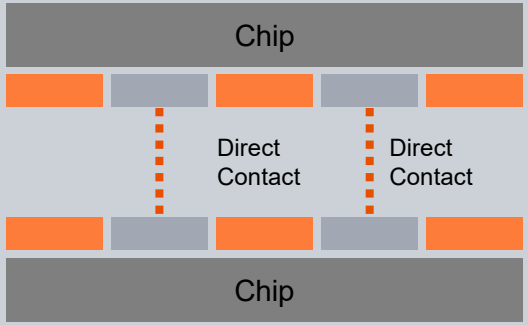
Supply of EUV optical equipment (Best case)

(Unit: Number of equipment delivered per year)



Source: ASML, PwC analysis

3D chip innovation

	TC bonding	Hybrid bonding
Definition	Microbumps between chips limit height reduction during stacking	Reduces gap between chips; Essential for many-layer stacking
Bonding method		
Key challenges	Bonding heat causes microbumps to melt and spread	The equipment cost is 4x higher than TC bonder

Demand for specialized back-end equipment is rising, and hybrid bonding has emerged as a cornerstone of multi-die stacking. Traditional thermo-compression (TC) methods rely on ~40-µm micro-bumps, limiting I/O density and adding resistance as layer counts grow. Hybrid bonding, in contrast, forms direct Cu-to-Cu contacts at sub-10-µm pitch, enabling higher bandwidth and a flatter stack.

The technology is challenging perfectly clean, plasma-activated surfaces and tightly controlled roughness are mandatory for void-free bonds. Besi currently leads commercial supply, with more than a hundred tools shipped and capacity expansion under way, but as HBM and logic-on-memory stacks ramp, tool availability could tighten.

Competition is building. EV Group is shipping wafer-to-wafer hybrid bonders, while ASMPT, Hanmi and others are developing die-to-wafer systems. Several IDMs are also pursuing in-house platforms. Unlike EUV lithography—which remains a near-monopoly—hybrid bonding is more likely to see multiple qualified suppliers before the decade ends, accelerating 3D integration across the industry.

Stronger materials, longer runs

As node sizes shrink, and packages grow more complex, legacy materials are bumping into physical and reliability limits. Copper lines suffer rising resistivity below 20 nm; traditional SiO_2 dielectrics inflate RC delay; and high-temperature plasma steps erode film uniformity. These effects blunt the power-performance-area (PPA) gains that once came “for free” with each new node.

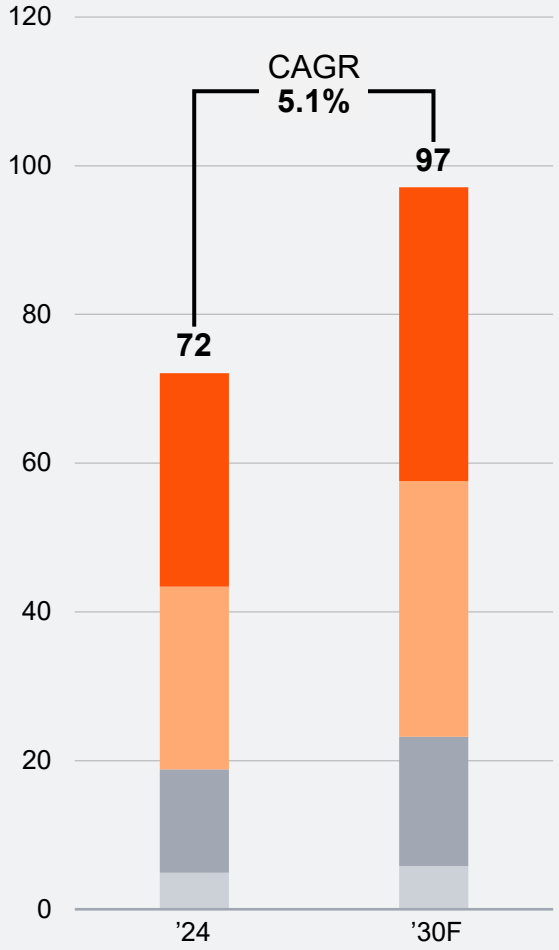
Meanwhile, manufacturing environments demand films that survive hotter anneals, harsher chemistries and sub-Ångström uniformity. Conventional etch and deposition chemistries are nearing their control limits, raising variability and threatening yield.

To push past these barriers, the industry is turning to new material sets. Cobalt, ruthenium and other alternative metals can have lower line resistance and stronger electromigration tolerance for next-generation interconnects.

High-mobility channels such as SiGe, strained Ge and III-V compounds are under evaluation for sub-2 nm transistors, while ultra-low-k dielectrics and engineered air gaps slash capacitance between wires. In advanced packaging, high-thermal-conductivity under-fills and novel redistribution-layer alloys improve heat spread and reliability in 3D stacks.

Looking ahead, material innovation can be as pivotal as lithography or design in sustaining Moore-scale progress. Foundries and suppliers that master these new chemistries can set the pace for the next era of semiconductor performance and manufacturability.

Semiconductor materials market forecast (Unit: $ Billion)



CAGR, 2024-30F

Fabrication material	+5.5%
Packaging material	+5.8%
Silicon wafer	+3.8%
Consumable parts	+2.7%

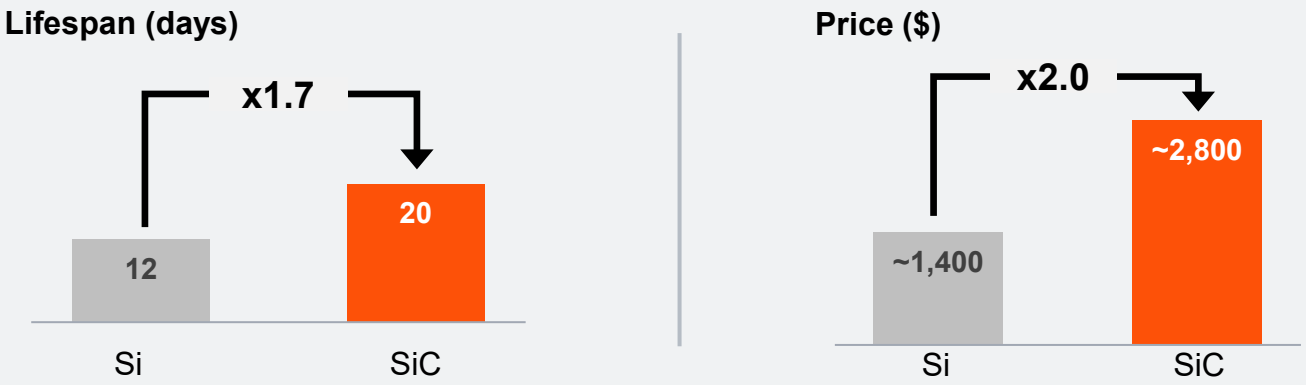
Source: Company announcements, Expert interview, PwC analysis

New materials, better chips

Plasma-facing parts such as focus rings, chamber liners and electrostatic-chuck plates have long been machined from silicon, but at today's higher plasma densities these components erode quickly and release particles. Foundries are therefore switching to silicon-carbide (SiC), whose much higher hardness and plasma resistance can extend part life by several multiples. Leading fabs report fewer unplanned stops and lower cost of ownership because SiC parts need far less frequent replacement.

Even harder candidates like boron-carbide (B_4C) are under evaluation; they can show still longer lifetimes but bring machining difficulty, higher cost and potential particle issues that must be solved before broad rollout. The common theme is clear: upgrading from Si to advanced ceramic carbides is becoming essential for keeping next-generation etch equipment running at peak utilization.

Impact of replacing focus rings components



Source: Expert Interview, PwC analysis

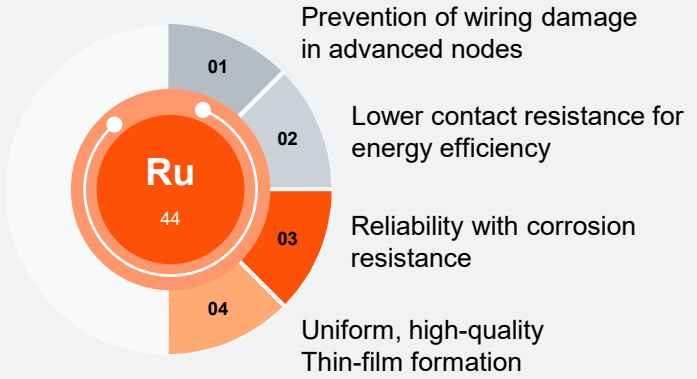
Next-generation interconnects

Below 7 nm, copper interconnects turn fickle: they thin out, slow down, and fail sooner from electromigration. Extra barrier layers prevent copper leakage but narrow the wires further.

A better fix is to replace copper with ruthenium—or coat it with a thin Ru layer. Ruthenium needs almost no barriers, carries current more easily in nanoscale lines, and can resist wear longer.

With scaling below 5 nm chips set to multiply quickly, ruthenium interconnects have potential to become a staple of the next wave of high-performance processors.

Ruthenium alloy benefits

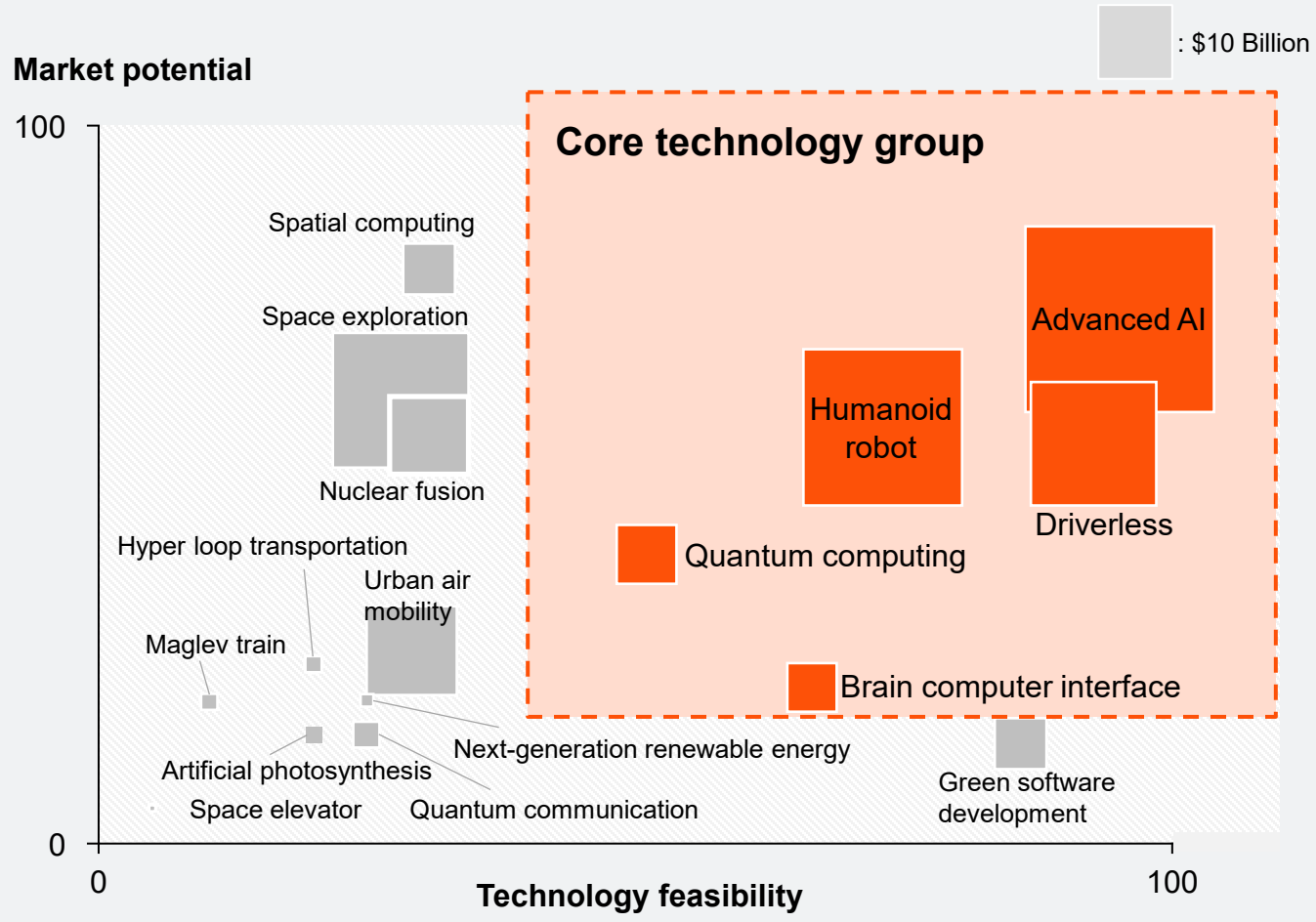


4

What’s Next?

Opportunities in semiconductor : AI and beyond

Major technological innovation beyond 2030



1) Scores are calculated by converting each element into relative index from 0 to 100.
Source: PwC analysis

Semiconductors will likely remain crucial in driving technology innovations beyond 2030. We've analyzed technologies with strong ties to semiconductors, evaluating their growth potential and feasibility. This analysis is designed to help the semiconductor industry prepare for its vital role in future advancements.

Methodology[1)]

Technology feasibility score (X-axis)

- Feasibility readiness (commercialization timing)
- Incremental investment over the most recent 5 years
- The number of doctoral graduates in relevant fields

Market potential score (Y-axis)

- Expected semiconductor market size in the year 2030
- Semiconductor market CAGR from 2024 to 2030

Investment scale (Size)

- Total investment on the technology over the past 5 years

Advanced AI

What will the limit of artificial intelligence be? The road to achieving artificial general intelligence and the role of semiconductor as the future unfolds.

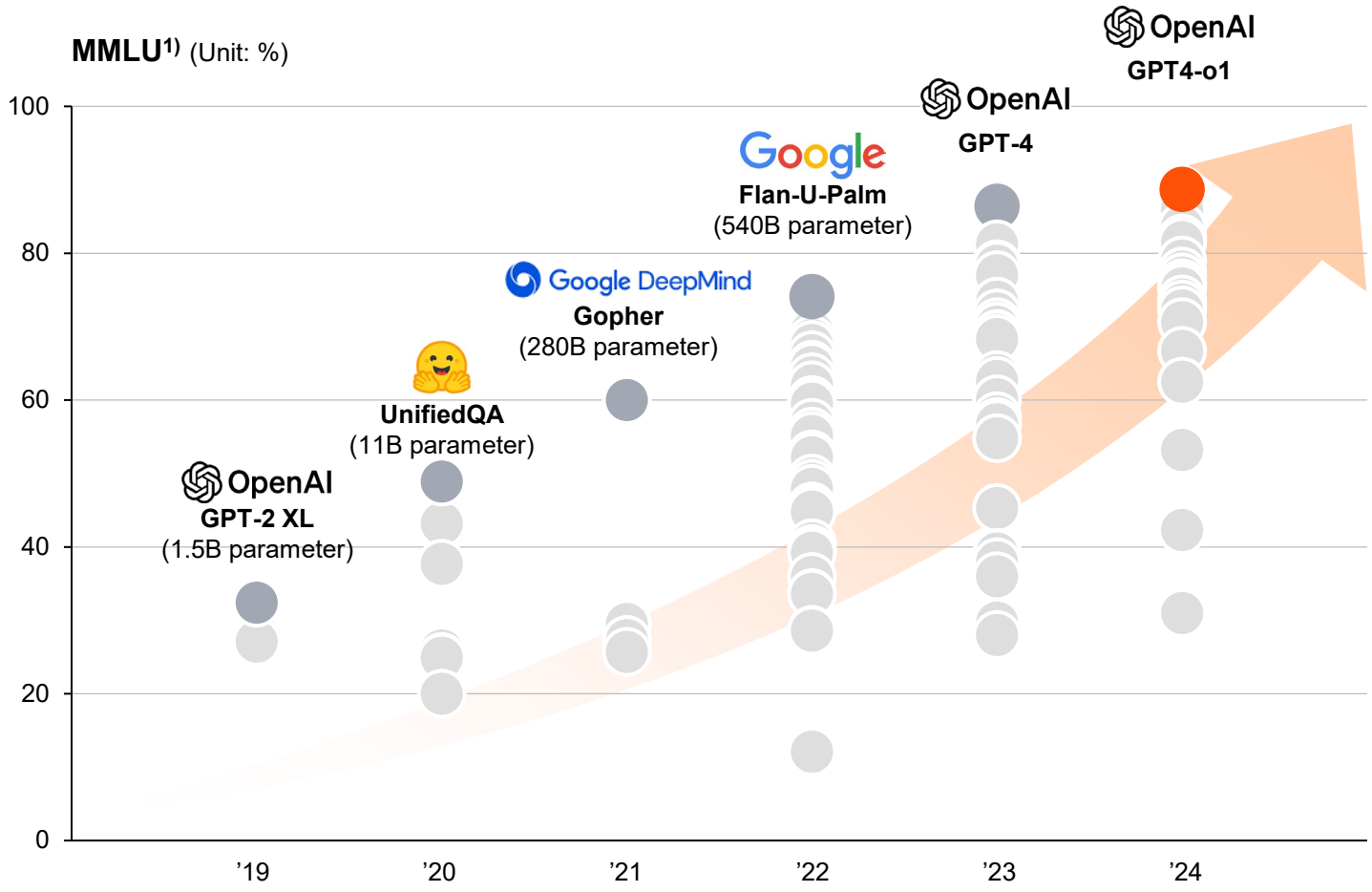
Market potential score

Proven rapid growth bringing financial value across various industrial applications. Growth momentum is expected to continue.

Feasibility score

Technological investments and a rising pool of skilled talent are driven by increased demand from end applications. Partial artificial general intelligence (AGI) is anticipated within 2 to 5 years, with a complete AGI expected in over 10 years.

Performance benchmark of major Large-Language Models (LLMs)



1) MMLU stands for Massive Multi-task Language Understanding, often used as a benchmark to measure general knowledge each AI model acquired. This graph is based on the data of published papers
Source: PaperswithCode

As of 2024, AI already outperforms humans on several headline benchmarks—for instance, topping human accuracy on ImageNet image classification and achieving higher scores on certain English-reading tests—and the pace of improvement continues to rise every day. From the outset, many AI researchers have pursued systems that match or exceed human-level intelligence. That recent progress has drawn record levels of funding and talent into the field.

Today, teams are both refining domain-specific large language models (DS-LLMs) that contain deep expertise in narrow subjects and pushing toward the longer-term ambition of artificial general intelligence (AGI), which would handle a far broader range of tasks with greater autonomy. Along the way, stronger AI capabilities spur new applications, those applications can attract more investment, and the cycle repeats—fueling still faster progress toward DS-LLMs and, ultimately, AGI.

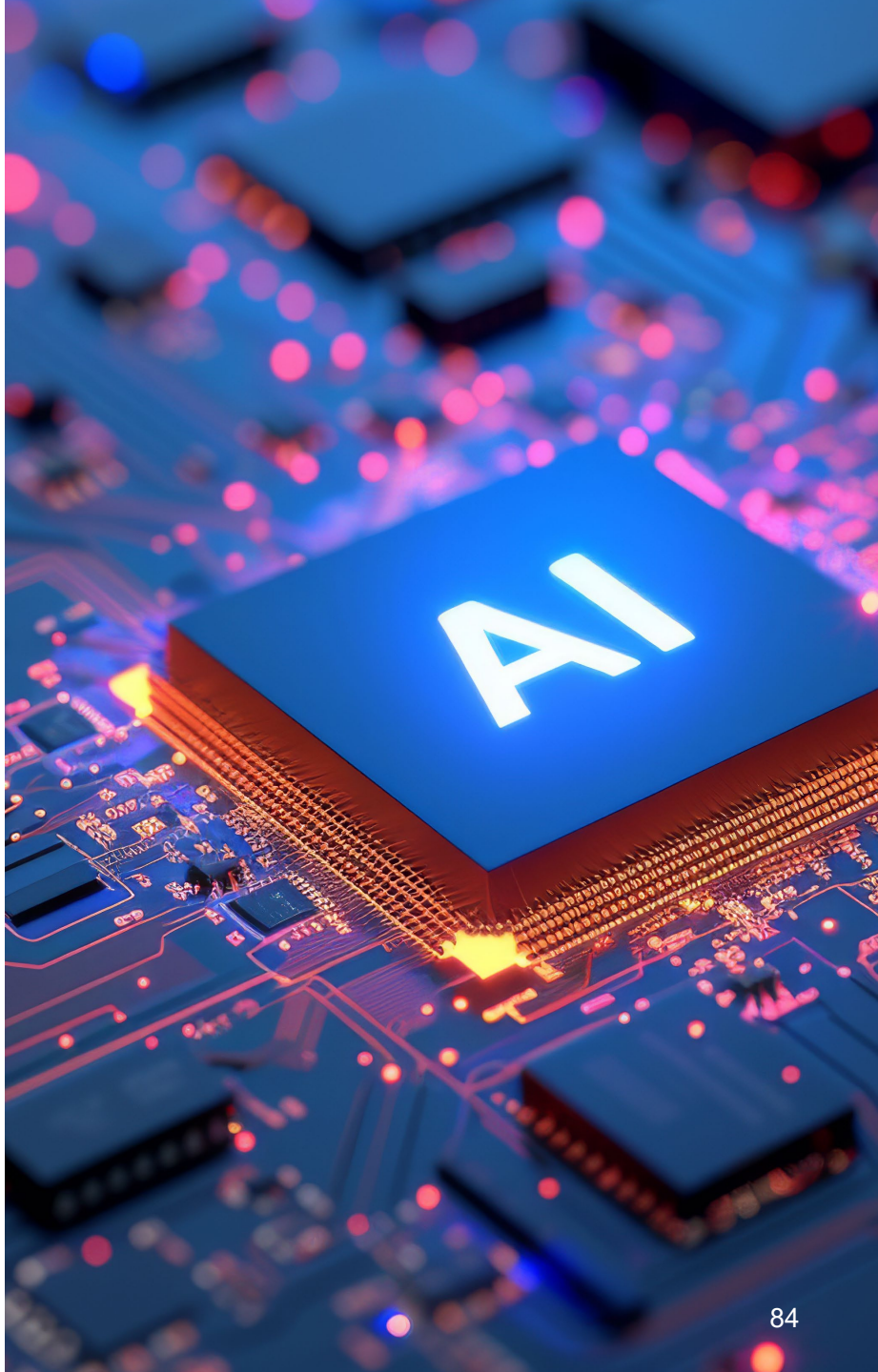
Semiconductors on the road to AGI

AI's progress is limited less by algorithms than by two practical hurdles: the need for vast, high-quality data and the computing muscle to process it. Investment is pouring into both areas, spurred by clear evidence of AI's value.

Pursuing artificial general intelligence can hinge on next generation semiconductors. Ever-larger models demand faster, more efficient logic dies built on smaller nodes and linked with high density 2.5D or 3D packaging. At the same time, high-bandwidth, low-latency memory can be essential for moving and storing the massive datasets used in training.

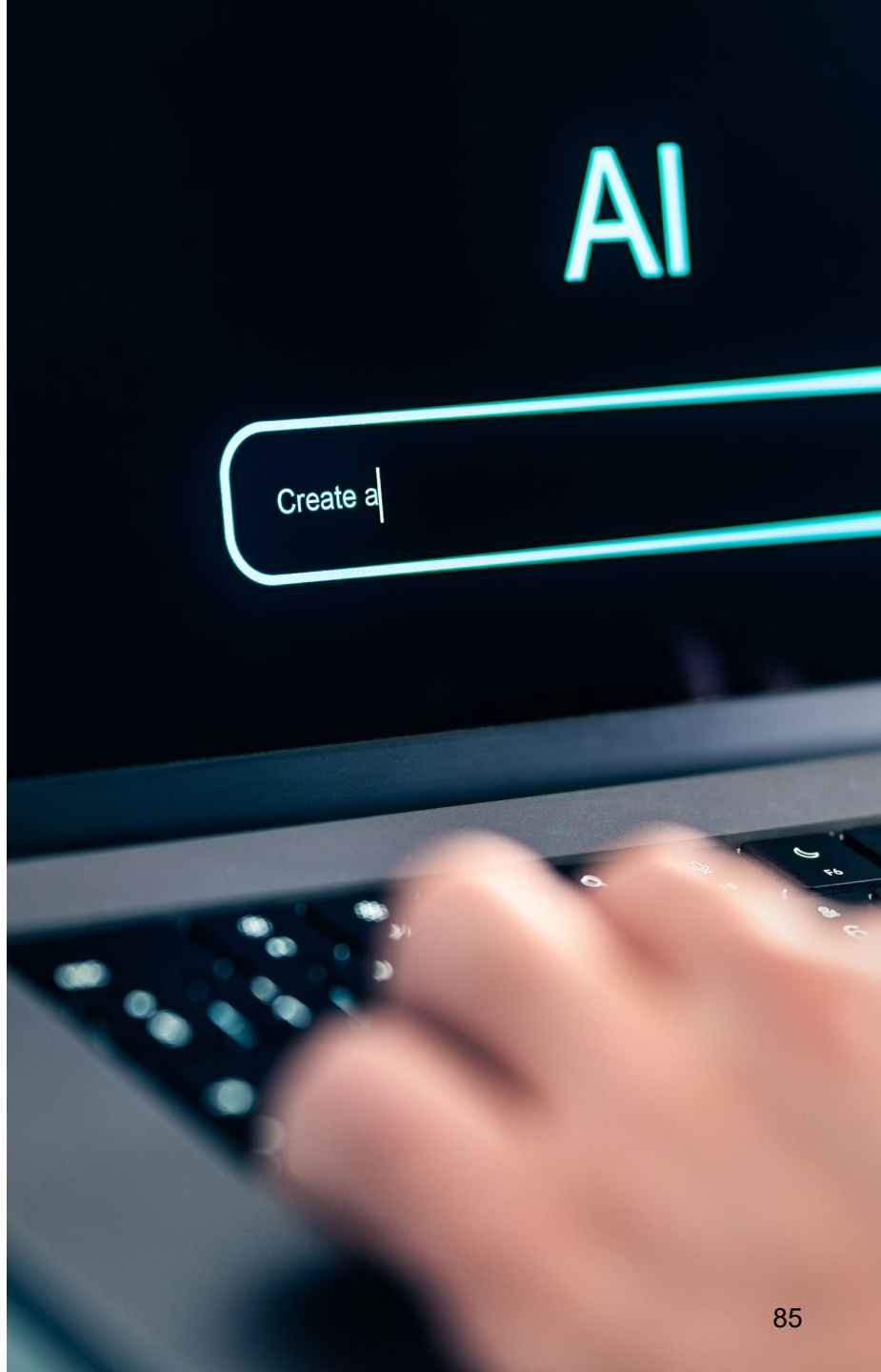
R&D is also shifting toward neuromorphic and in-memory approaches. Domain-specific NPUs already ship in edge devices, and processing-in-memory (PIM) prototypes place compute elements beside—or inside—DRAM arrays, shrinking data-movement energy and delay. Fully neuromorphic hardware, which mimics the brain's architecture, may require fresh device concepts plus advanced packaging, but it can bring dramatic gains in compute per watt and per cubic centimeter.

Taken together, these semiconductor advances form the backbone of the journey from today's specialized AI to tomorrow's more general, capable intelligence.



Charting the path forward

- Choosing between custom and off-the-shelf silicon : Weigh the trade-offs of a custom AI accelerator versus standard GPUs or CPUs. Factor in model size, algorithm complexity, power limits, and the value of faster time-to-market.
- Aligning product roadmap : AI demand spans many sectors, so track breakthroughs—and supply constraints—in high-performance chips. Time your adoption to when new nodes or packages give a clear competitive edge.
- Building a resilient supply chain : Advanced, low-power devices such as NPUs or PIM arrays need long lead times before volume ramps. Secure capacity early and cultivate deep partnerships to smooth future shortages.
- Integrating next generation designs : Stay current with new design flows, develop both hardware and software, and collaborate across the value chain to hit strict energy efficiency and performance targets as the industry moves toward AGI.



Driverless future on wheels

Major automotive and tech companies are embarking on what may be their most important transformation of the next decade

Market potential score

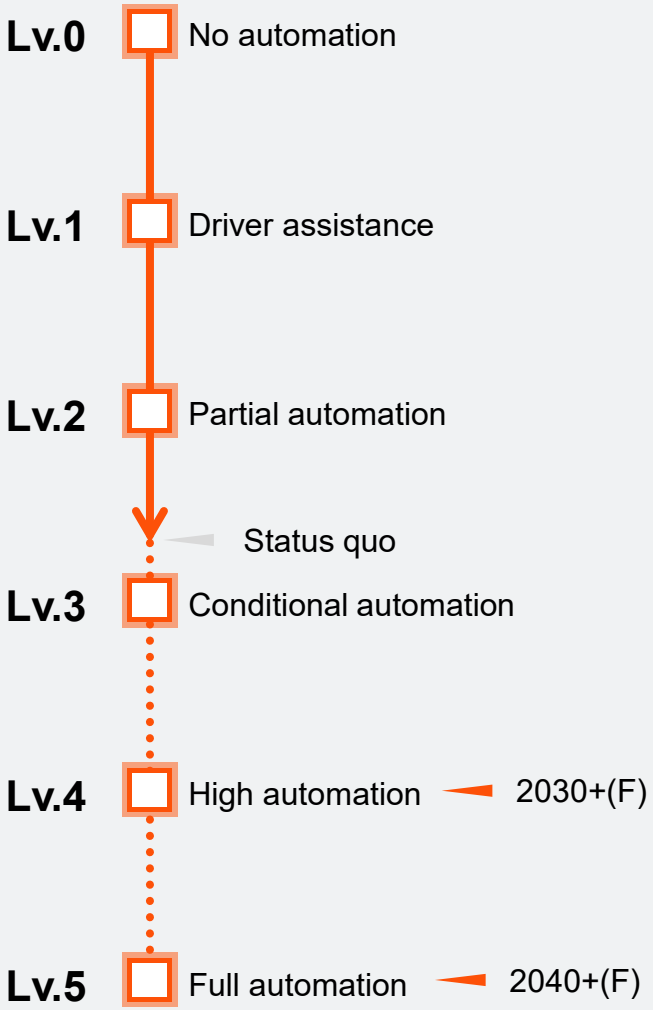
Low High

Demand for sensors, AI processors and power devices can keep climbing as more new cars ship with high-level autonomy by the 2030s, making semiconductors central to future mobility.

Feasibility score

Low High

Level 4 pilot fleets already operate in geo-fenced zones. Broader rollout hinges on safety data, regulation and cost, so mass adoption may still be a few years away.



How close are we to fully autonomous driving?

- The autonomous level of vehicles runs from level 0 to level 5. Most production cars today are level 2—they steer and brake themselves in defined scenarios but still need a human in the loop. Only a handful of pilot models offer level 3 hands-free driving on specific highways. Several automakers and tech firms are testing level 4 robo-taxis in geo-fenced areas, yet level 5 (go anywhere, no human fallback) remains out of reach.

What technologies are needed for full autonomous driving?

- On-board systems: high-performance compute SoCs, multi-modal sensor suites (camera, radar, LiDAR), robust software stacks, precise GNSS and HD maps.
- Infrastructure: low-latency 5G/6G networks, edge/cloud data hubs, road-side vehicle-to-everything (V2X) units and smart road sensors for real time traffic data.
- Regulation and standards: safety certification, cybersecurity rules, common communication protocols and clear liability frameworks.

When could full autonomy be commercialized?

- Many experts expect limited level 4 services (robo-taxis or hub-to-hub freight) to scale in select cities by around 2030. Level 5, which can handle most of road and weather condition without a steering wheel, is likely to arrive much later—well into the 2040s or beyond.
- Besides technical hurdles, legal, ethical and social issues may shape the timeline, and progress can vary by region, infrastructure readiness and public acceptance. Early roll-outs can probably appear first on controlled highways or tightly mapped urban cores.

How will autonomous vehicles transform the semiconductor industry?

When fully autonomous vehicles are commercialized, the number of semiconductors required per vehicle may increase, thereby expanding the market. Currently, conventional vehicles on the market typically contain about 200 to 300 semiconductors.

In contrast, autonomous vehicles at level 3 and above, which do not require a driver to take the wheel, could need more than 1,000 semiconductors. As development progresses towards full autonomy, significant changes in market size are anticipated.

Currently, automotive semiconductors are primarily used for engine control, safety systems, and infotainment systems. However, in autonomous vehicles, apart from these traditional uses, high-performance semiconductors can be required for data processing, AI computation, and real-time network connectivity. Particularly, with the advancement of autonomous driving capabilities and the enhancement of communication and AI functions, the demand for high-performance computing chips such as domain control units (DCUs) and sensors, as well as communication chips for V2X, is expected to grow substantially.

As the number of semiconductors in these vehicles increases, packaging methods may also become more advanced, transitioning from single-chip solutions to chiplet architectures.

Additionally, the value chain for automotive semiconductor production can also change. For levels 0 to 2 of autonomous driving, industry-standard chips have provided sufficient performance. However, for higher levels of advanced autonomous driving, specialized chips tailored to each company will likely be necessary. This can result in more instances of OEMs designing and producing their own chips.

Charting the path forward

- Preparing software and hardware capabilities: As autonomy rises, software that orchestrates sensors and compute hardware becomes mission-critical. OEMs, Tier 1s and chip suppliers must forge strong alliances to enable system level compatibility and over-the-air upgrade paths.
- Securing in-house production capabilities: A growing number of automakers are designing their own SoCs for central compute, digital cockpit, ADAS and even LiDAR signal processing. Each OEM needs a clear strategy; stay with the traditional supply chain, adopt vertical integration, or choose a hybrid approach—defining just how much design and manufacturing to bring inside the company.

Humanoid robot

The emerging era of robotics, powered by AI and autonomous technology, can open another big market for semiconductors.

Market potential score

Low — High

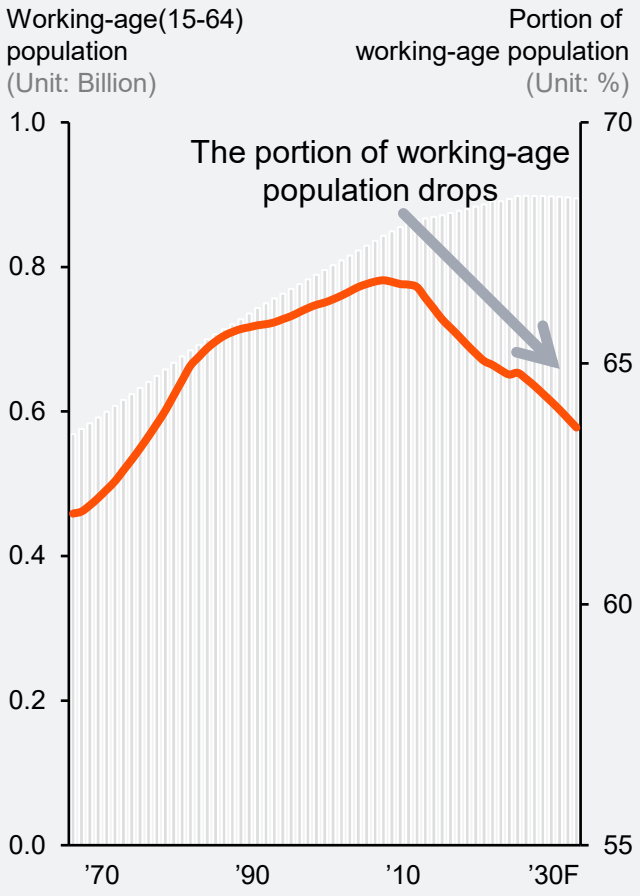
The robotics market size is large, as robots are widely applicable across industries. Studies on complex movements are underway, with increasing demand due to labor shortages that can fasten growth with repeated technological advancements.

Feasibility score

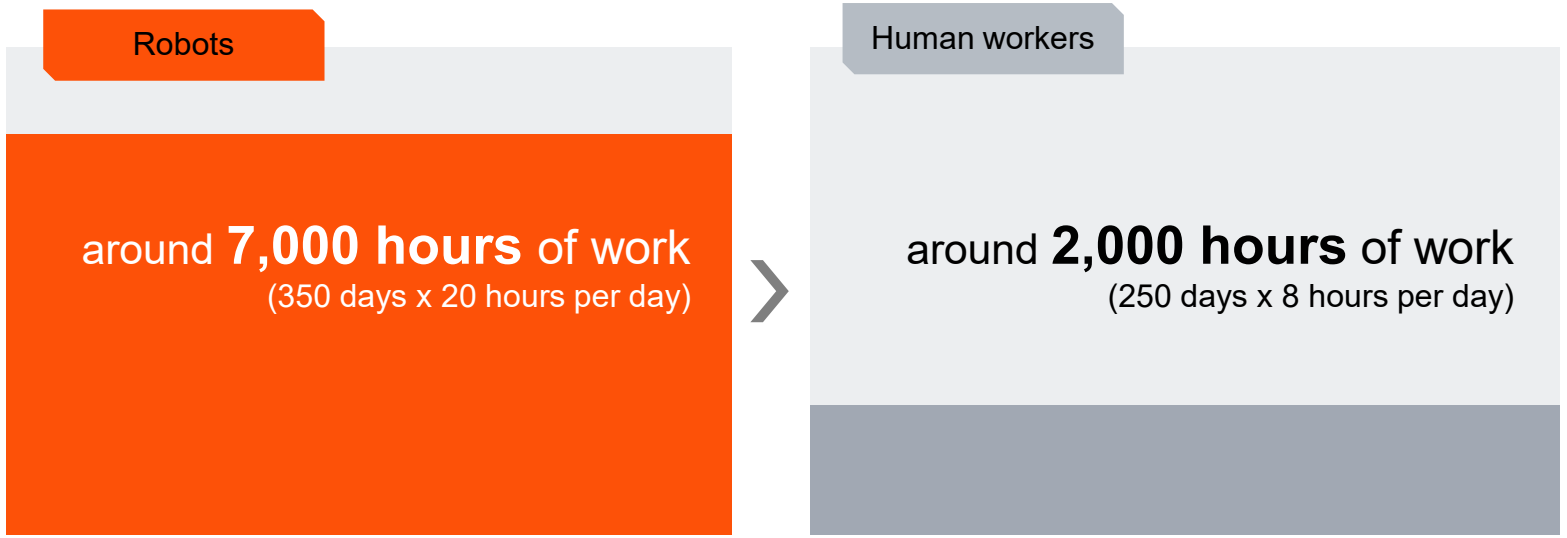
Low — High

Related investment has peaked before 2023 and is stabilizing. It's expected that humanoids can be commercialized with continuous R&D by key startups backed by large corporations.

Working-age population of OECD countries



Source: Worldbank



As the global population ages, labor shortages are becoming a major challenge, especially in developed countries. Robotics technology has continued its own innovation and is now being recognized as a game-changer to solve labor shortages and enhance human productivity. Calculated simply, robots can operate around the clock with low downtime, delivering around 3 times more working hours than a human.

So, which types of robots are expected to see the most growth in the future? Industrial robots have already entered a stable growth phase, expanding their presence. Service robots—like air purification and restaurant serving robots—are also growing fast, expected to accelerate their use cases to senior healthcare, security, pet care, and much more.

A noteworthy area on the rise is humanoid robots that integrate AI and autonomous technology. These robots are evolving beyond simple hand movements, advancing to a level where they can replicate complex actions like basketball slam dunks. Beyond hardware innovation, software is also evolving with AI and AGI, enabling robots to learn autonomously in real time. In the near future, robots may permeate businesses and households in countless forms, transforming the way we live.

Source: PwC analysis

Semiconductors are the blood, bones and muscles of humanoids

Robotic technology is evolving rapidly, and at the heart of its advancements lie semiconductors that enable sensing, data processing, decision-making, and the actions. In particular, the demand for processors, sensors, and MEMS is expected to surge in the coming years.

AI processors lie at the core of robotic intelligence, responsible for decision-making and real-time data analysis. These semiconductors can empower robots to autonomously process the data and operate without human interaction. With NPU-based edge computing, robots may also be able to independently function even in environments without a stable network connection, enabling seamless decision-making.

To integrate robots into our physical world, sensors play a crucial role. CMOS image sensors allow robots to "see" and interpret their surroundings, while ToF(time-of-flight) and LiDAR technologies enable precise 3D environmental mapping. Additionally, MEMS sensors help robots detect their own motion and physical condition, enhancing both accuracy and efficiency. These sensors, based on semiconductor technology, directly impact a robot's performance and reliability. Moreover, 5G and next-generation network technologies may enable that robots communicate faster and more securely. Lastly, PMICs and power semiconductors can enhance the stability of the robots, enabling them to efficiently control power and support humans for longer period of time.

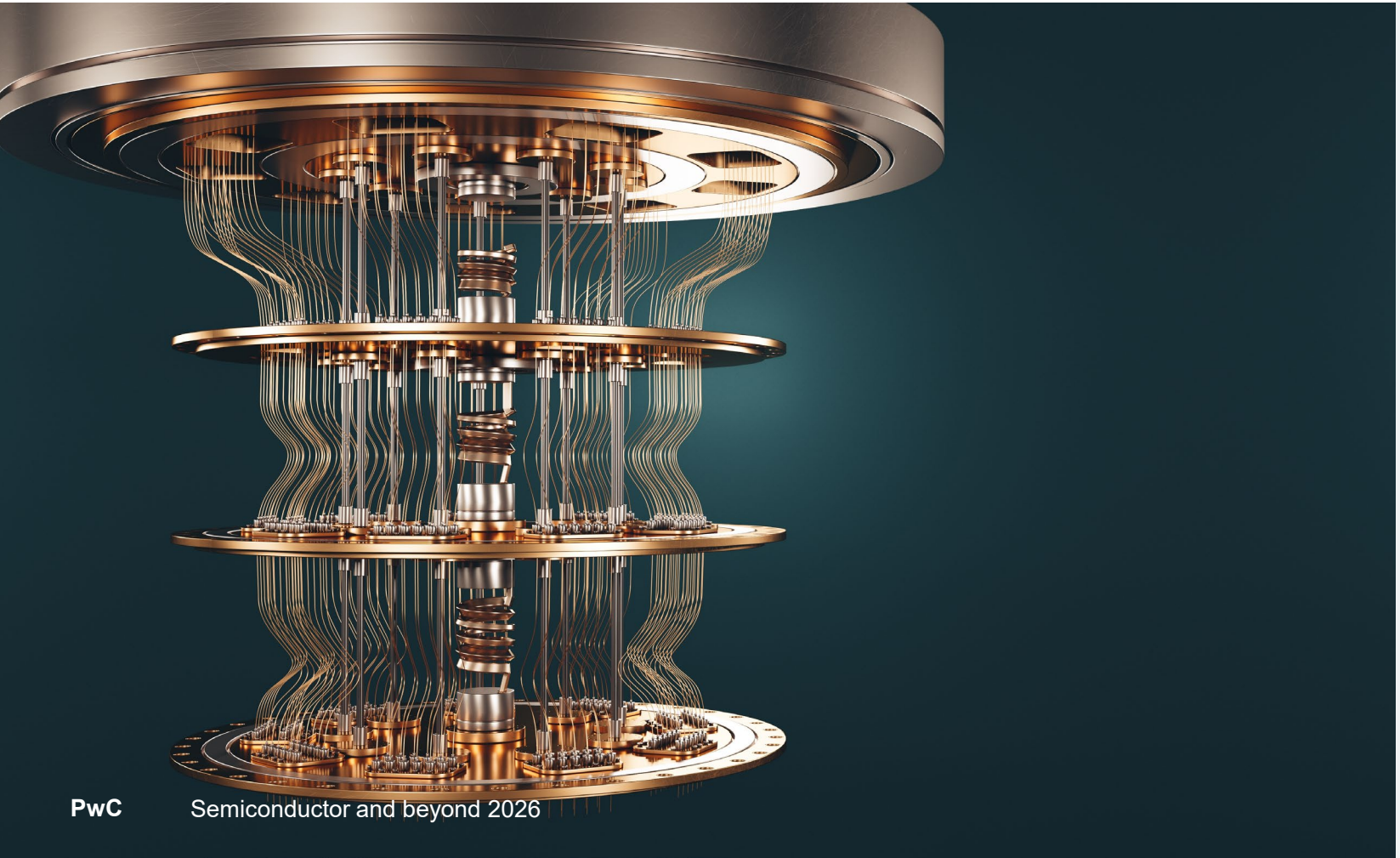
Simply put, the future of robotics is inseparable from semiconductor advancements. From processors acting as the "brains" to sensors providing signals and actuators and MCUs enabling movement, a big part of robotic function can depend on semiconductor innovations. Companies leading this technological frontier are driving the robotics industry forward, shaping a future where robots are deeply embedded in human life.

Charting the path forward

- Ecosystem Integration : Delivering AI features and seamless over-the-air updates can require tight hardware–software integration from the R&D stage. Forming strategic partnerships that enable cross-platform compatibility will likely be decisive in shaping market leaders.
- Energy consumption in mind: Battery-powered robots may pack ever more compute, creating heat-dissipation and power-management challenges. For last-mile delivery bots, drones and compact service robots—where frequent charging is impractical—achieving high energy and thermal efficiency is critical.
- Skilled workforce development: Demand for robotics-specific SoC designers already outstrips available talent. These devices can call for expertise in real-time processing, embedded AI and multi-sensor fusion, so attracting and cultivating such skills can be essential for sustained innovation.

Quantum computing

Quantum computing will be a key next-generation technology for tackling complex problem of the future



Market potential score

Low — High

Although the current market size is still modest, the growth rate is expected to be very high after commercialization. This technology could significantly impact areas such as security and finance, leading to a rapid expansion in demand under government leadership.

Feasibility score

Low — High

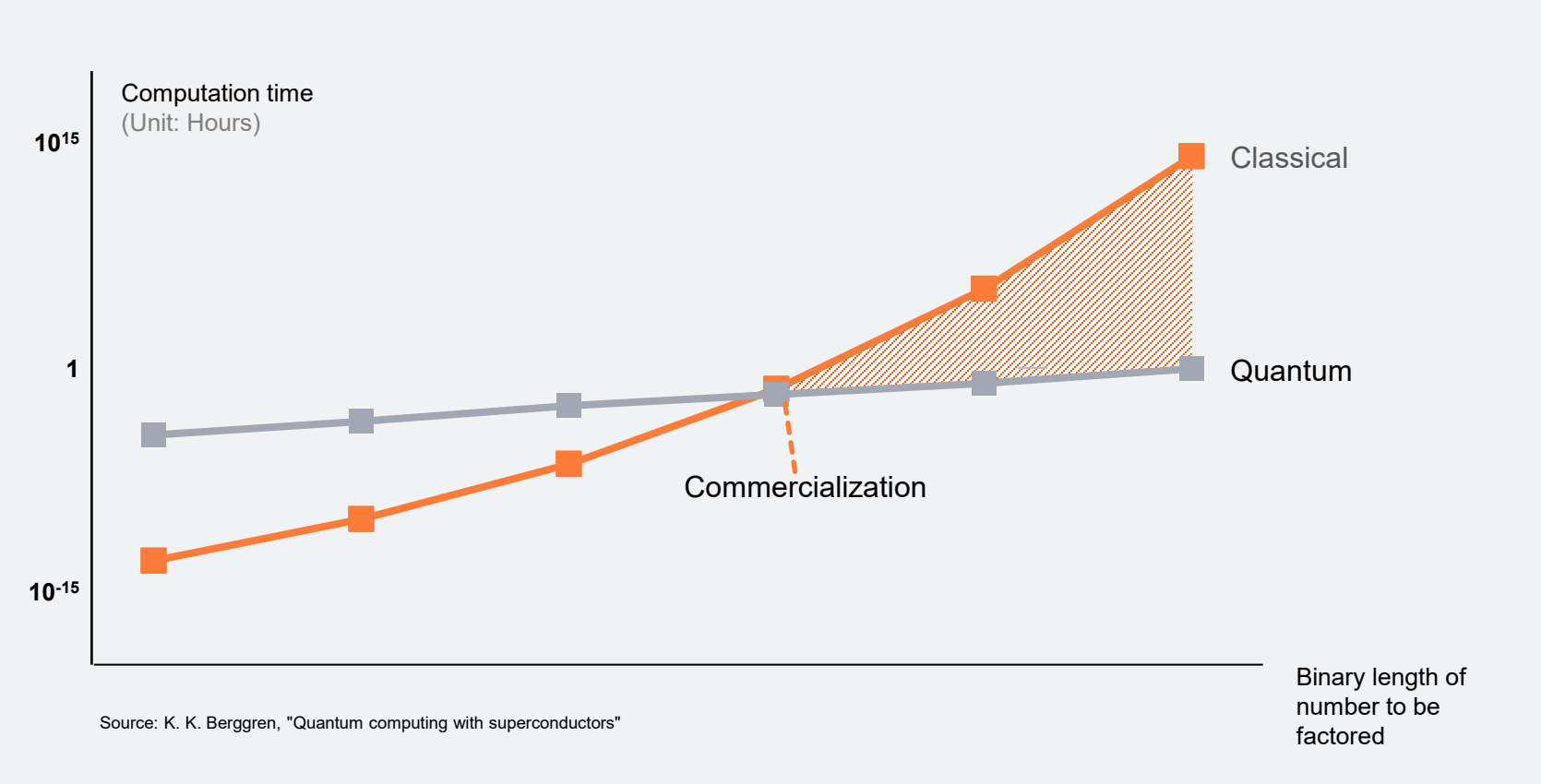
With the release of a new quantum processor to the market in early 2025, it is expected to be commercialized in a relatively short period of time.

The rise of quantum computers

A quantum computer uses the principles of quantum mechanics—superposition and entanglement—to explore many computational paths simultaneously, allowing it to tackle certain problems, such as large-number factorization, molecular simulation or complex calculation, far faster than classical machines.

Additionally, the gates and algorithms used in quantum computers, notably Shor's algorithm and Grover's algorithm, are noteworthy for dramatically improving information processing speed and having the potential to render many current encryption systems ineffective. Because of such breakthroughs, quantum computing is viewed as a future game-changer in fields like quantum chemistry, drug discovery, portfolio management and materials science.

Recognizing the strategic value, governments worldwide have named quantum technology a critical discipline and are funding R&D accordingly. Industry players— from IBM, Google and Microsoft to specialized start-ups such as IonQ, Rigetti and Riverlane—announced to scale from today's noisy-intermediate-scale processors to fault-tolerant machines with millions of error-corrected qubits.



Recent prototypes with hundreds of physical qubits suggest steady progress, yet meaningful commercial impact still depends on advances in qubit coherence, error correction and cryogenic control. Even so, the rapid pace of research is fueling expectations that practical quantum computing may arrive sooner than once thought.

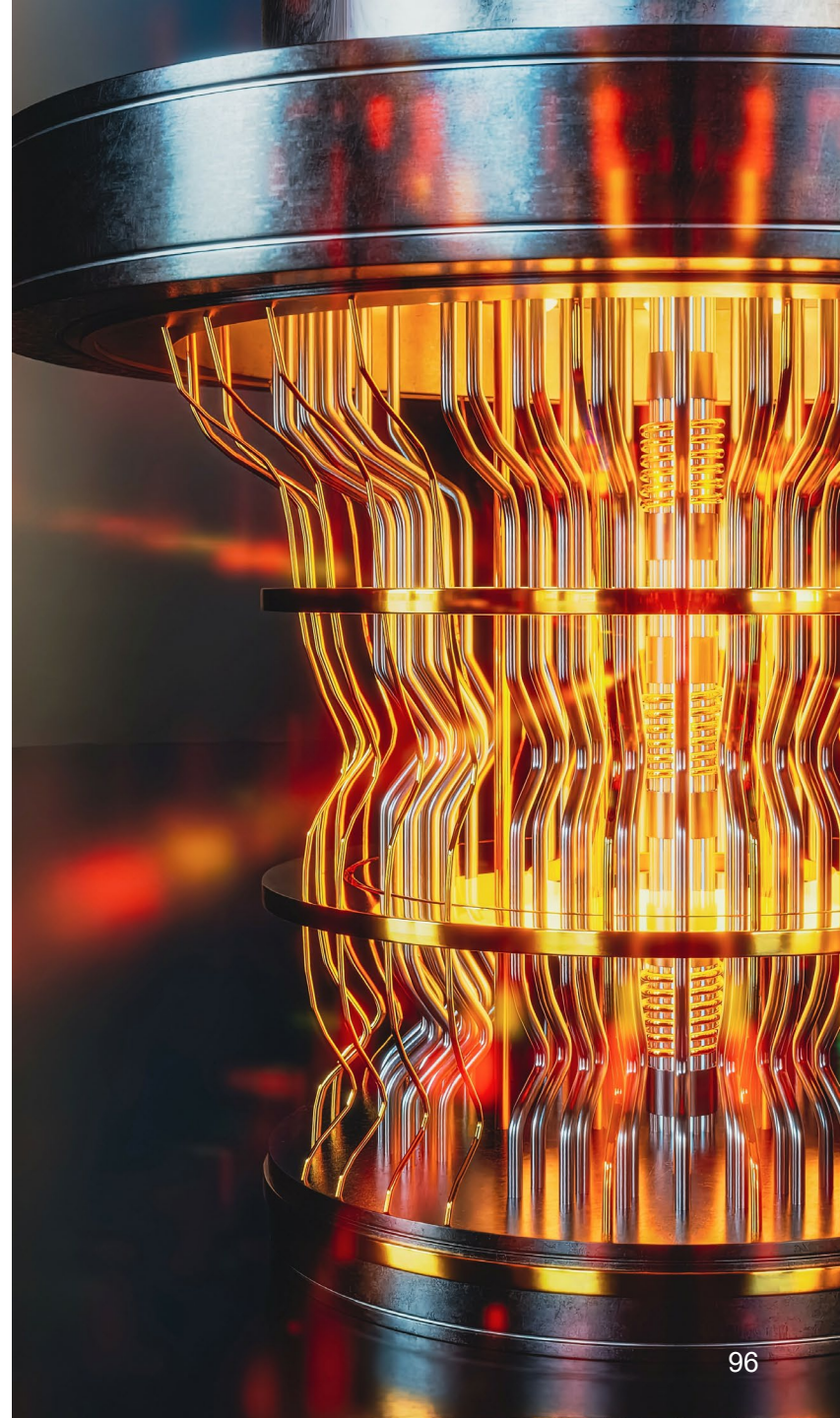
Will quantum computing replace silicon?

Quantum computers represent a novel technological frontier, yet in the short term, they may rely significantly on the conventional semiconductor chips we have been using. While they offer rapid computational capabilities, quantum computers also have vulnerabilities. These vulnerabilities stem from the unique superposition states inherent to quantum systems. Unlike classical bits, qubits can quickly decohere even with low noise. Therefore, to effectively utilize quantum computers, it is critical to develop technologies for stabilizing qubits and implementing quantum error correction(QEC) to rectify decohered qubits. Supercomputers are typically employed in these processes, giving rise to the current landscape of "hybrid quantum computing," which combines quantum computers and supercomputers.

In this context, there is a growing demand for semiconductors capable of executing complex QEC algorithms using the parallel computing capabilities of GPUs, as well as those that enhance data communication speed between quantum computers and supercomputers.

Consequently, when quantum computers reach commercialization—generally considered to be when they incorporate more than one million qubits—it may not lead to the decline of the existing silicon semiconductor market. Instead, silicon semiconductors may serve as integral components within quantum computers, fostering a mutually beneficial relationship that expands the market for both technologies.

These technologies can be applied in various areas, including solving complex problems in logistics and supply chain management, accelerating drug development through molecular simulations, enhancing cybersecurity through advanced encryption methods, and improving artificial intelligence and machine learning algorithms. In particular, there is a potential short-term threat to the financial and security industries due to the risk of existing encryption systems being compromised. This scenario is likely to spur proactive government-led investments in the development of these technologies



Charting the path forward

- Balancing quantum and classical resources : Fault-tolerant quantum systems can still rely on fast classical processors for error correction, scheduling and data pre/post-processing. Chip makers should align their roadmaps to supply low-latency control ASICs, cryo-compatible interfaces and high-bandwidth links that tie quantum modules to classical HPC clusters.
- The two camps of quantum computers : Quantum computing presents two paths, influencing semiconductor strategies. Superconducting qubits, which can leverage existing semiconductor processes offering high scalability, or trapped ions, which have relatively lower error rates and can operate at room temperature. Monitoring of these camps can guide semiconductor players find their position in this emerging field.
- Collaboration with government : Because the technology spans physics, materials and advanced manufacturing, pursuing national R&D grants, tax incentives and public–private partnerships can accelerate quantum-related semiconductor development while sharing risk.

Brain-computer interface

From neurological treatments to broader applications, semiconductors can decode and relay the brain's electrical signals

Market potential score

Low High

The initial target market may be limited in size, focusing on patients, but it's expected to grow rapidly as it moves past the basic research and enters the clinical-trial phase.

Feasibility score

Low High

Non-invasive BCI has already begun commercialization, with advancements in sensor and computing performance. Invasive types are also expected to be commercialized in the next five to seven years, with growing numbers of researchers interacting expertise in both healthcare and AI.

How a brain-computer interface works

01
Brainwave Sensing

02
Digitize analog signal

03
Signal processing and command

The human brain is the most complex organ in our body. When we see, hear, perceive, and make judgments, our brain generates electrical activity known as brainwaves. The effort to connect these brainwaves with computers is what brain-computer Interface (BCI) technology is about. This innovation aims to translate thoughts confined within our minds into external outputs and, conversely, allow external signals to influence the brain. This holds great potential, particularly for individuals with paralysis, sensory impairments, or neurological disorders.

Although you might think BCI is like a science fiction story for superhumans, BCI research began in the 1970s and invasive (implant) technology like deep brain stimulation (DBS) is already in use to treat epilepsy. This method delivers electrical impulses to certain brain regions when seizures occur. Since the late 2000s, both invasive and non-invasive BCI devices have advanced through clinical trials

Nowadays in some countries, trials of invasive BCI have started, and successful trials have documented restoration of movement and communication in paralyzed patients. Implantation methods such as the vascular method are also emerging to reduce surgical risks.

Non-invasive BCI, though less precise, is more accessible, advancing at its own pace as well. EEG (Electroencephalogram)-based technology enables users to control robotic prosthetics, track stress levels, and even interact with games with brainwaves. Some of these devices have already received FDA certificates and are being commercialized.

Though not yet mainstream, BCI is rapidly evolving, with applications expanding in healthcare, assistive tech, and entertainment. With ongoing breakthroughs, a future of thought interaction with machines may be closer than ever.

Advanced, custom, and low-power for BCI

The concept of BCIs relies on electrodes to detect brain signals and electronic circuits for communication between the brain and external devices. As our brainwaves are a massive and extremely complicated data input, processing this data from the brain can require advanced, ultra-low-power AI accelerators, analog-to-digital converters, and amplifiers. This is also important in non-invasive BCIs, where the signals are weak and need precise amplification.

For invasive BCIs, since they are often implanted for a long time, it's crucial to reduce their size, heat, and power consumption. Using biocompatible materials and packaging methods is also essential for the safety and functionality within the body. Therefore, the demand for ASICs tailored for BCI can increase.

To process the digitized brain signals with low-latency, there can be an increasing demand for SoCs including AI accelerators and digital signal processors (DSPs). These chips interpret data and turn them into intent and actions, requiring advanced chips capable of low-latency performance.

Additionally, transmitting brain signals to external receivers involves low-power, short-distance communication chips such as RFIC or low-power Bluetooth-low-energy (BLE).

Last but not least, the BCI market may also increase the demand for devices act on the brain signals—such as gaming handhelds, monitors, and robotic prosthetics. This can drive the demand for network chips, GPUs, AI accelerators and SoCs that can handle both graphical computations and signal processing. The market for advanced, custom, and low-power semiconductors can grow over time, as BCI expands its application from medical use to healthcare, and entertainment.

Charting the path forward

- Prioritizing security : Since BCIs handle highly sensitive neural data, security technology will likely be a competitive edge. Chip design must integrate data protection mechanisms at the early stage, defining key protection areas and incorporating encryption capabilities within SoC to prevent unauthorized access.
- Aligning with regulatory changes : Invasive BCIs, which involve direct implantation into the body, require even more rigorous safety validation from the government. This involves designing chips that not only comply with regulations such as those from the FDA but also pass stringent safety validation processes. Companies must remain up-to-date on regulations and evaluate their impact on chip-level design for successful market entry.
- Facilitating software compatibility : Seamless integration between hardware and software is a must for BCI applications to enable reliable interaction with downstream devices and user interfaces. Companies should work closely with ecosystem partners to enhance interoperability from chip design to system implementation.

References

1. PwC, ”State of the semiconductor industry”, 28 Nov 2024
2. Bloomberg intelligence, "EV Share of Total Vehicle Sales"
3. PwC, The monthly Autofacts® Market Update
4. Economic Review, "Power Semiconductor takes more than 50% of EV components, Korea has still long way to go", 23-Dec 2015
5. Trendforce, "[News] Global GaN Power Device Market Size Expected to Reach USD 4.376 Billion in 2030, CAGR of 49%", 16 Aug 2024
6. Yole Group, "SiC and GaN: an industry driven by different engines", 15 Dec 2022
7. IEA, Electricity 2024, Analysis and forecast to 2026, Jan 2024
8. IDC, "Worldwide Wi-fi Technology Forecast Update, 2024–2028", Mar 2024
9. Ericsson, "Ericsson Mobility Report", Nov 2024
10. Analog Devices, "GaN Power Solutions"
11. Statista, "Market: Household major appliances worldwide", 2019-2029
12. Statista, "Market: Consumer Service Robotics worldwide" & "Market: Gaming Equipment - VR Headsets worldwide", 2018-2029
13. Statista, "Market: Telephony - Smartphones worldwide", 2018-2029
14. Statista, "Market: Consumer Electronics - Computing worldwide", 2018-2029
15. Gartner, AI PC Unit Shipments, Worldwide, 2021-2027
16. Gartner, GenAI Smartphone Unit Shipments, Worldwide, 2021-2027
17. Statista, "Medical Devices - Worldwide", Aug 2024
18. Gartner, IoT Endpoints and Communications Forecast, 2Q23
19. IEA, "Renewables 2024, Analysis and forecasts to 2030", Oct 2024
20. Statista, "Renewable energy market size worldwide in 2021, with a forecast for 2022 to 2030", Dec 2022
21. KIET, The Impact and Implication of the Russia-Ukraine War on Global Defense Market, Mar 2023
22. Fry BT, Howard RA, Thumma JR, Norton EC, Dimick JB, Sheetz KH. Surgical Approach and Long-Term Recurrence After Ventral Hernia Repair. JAMA Surg. 2024;159(9):1019-1028. doi:10.1001/jamasurg.2024.1696
23. Infineon, "Wide Bandgap Semiconductors (SiC/GaN)"
24. NVIDIA, NVIDIA Data Center GPU Resource Center
25. IBS, Costs to produce a new chip, 2018
26. SEMIWIKI, Interface IP in 2022: 22% YoY growth still data-centric driven, Apr 2023
27. Synopsys, 2024 Annual Report, 2024
28. Cadence, 2024 Annual Report, 2024
29. SIEMENS, 2024 Annual Report, 2024
30. Gartner Forecast: Foundry Supply and Demand, Worldwide, 2005-2024
31. SEMI, World Fab Forecast, 2024
32. Omdia, PwC White paper on state of Semiconductor Industry
33. Gartner Forecast: DRAM Market Statistics, Supply and Demand, Worldwide, 2009-2028
34. Gartner Forecast: NAND Flash Supply and DemandWorldwide, 2009-2028
35. Yole Group, Power GaN: harnessing new horizons, Apr 2024
36. Yole Group, SiC and GaN: an industry driven by different engines, Dec 2022
37. Paul McWilliams, "Moore's Law is Dead - Long-live the Chiplet!", SemiWiki, 30 Sep 2022
38. Mark Lapedus, "Transistors Reach Tipping Point At 3nm", Semiconductor Engineering, 23 Feb 2022
39. Anton Shilov, "TSMC's wafer pricing now $18,000 for a 3nm wafer, increased over 3X in 10 years: Analyst", Tom's Hardware, 5 Jan 2025
40. Liz Allan, "Asia Government Funding Surges", Semiconductor Engineering, 18 Nov 2024
41. Trendforce, "[News] Global Developments in Advanced Packaging Projects", 27 Nov 2024
42. Invest Korea, “Strategy for Nurturing High-tech Industries by Sector”
43. SK Hynix, "[Understanding Semiconductors Part 7] AI Era, Packaging Technology Moving to a New Dimension! Chiplets and 3D SoC (7/7)", 29 Nov 2023
44. Gartner, IoT Endpoints and Communications Forecast, 2Q23
45. ASML, Annual Report 2022-2024
46. MarketScreener, "BE Semiconductor Industries N : Hybrid Bonding Presentation March 2022", Mar 2022
47. National Center for Science and Engineering Statistics, Survey of Earned Doctorates (SED) 2023, Sep 2024
48. PaperswithCode, "Multi-task Language Understanding on MMLU", Accessed 27 Feb 2025
49. Worldbank Databank, "Health Nutrition and Population Statistics: Population estimates and projections", 16 Dec 2024
50. K. K. Berggren, “Quantum computing with superconductors,” in Proceedings of the IEEE, vol.92, no.10, pp. 1630-1638, Oct. 2004, doi: 10.1109/JPROC.2004.833672.
51. Kawala-Sterniuk, Aleksandra et al. “Summary of over Fifty Years with Brain-Computer Interfaces-A Review.” Brain sciences vol. 11,1 43. 3 Jan. 2021, doi:10.3390/brainsci11010043

Authors

PwC Global Semiconductor Leader

Glenn Burm
Partner,
glenn.b.burm@pwc.com

Korea

Yoo-Shin Chang
Partner,
Strategy& Korea
yoo-shin.chang@pwc.com

Tommy Lee
Partner,
Strategy& Korea
tommy.lee@pwc.com

Tae-Young Kim
Partner,
Strategy& Korea
ty.kim@pwc.com

Seung-Wook Han
Partner,
Strategy& Korea
seung-wook.han@pwc.com

EMEA

Tanjeff Schadt
Partner,
Strategy& Germany
t.schadt@pwc.com

Steven Pattheeuws
Partner,
PwC Netherlands
steven.pattheeuws@pwc.com

India

Mohammad Athar Saif
Partner,
PwC India
mohammad.athar@pwc.com

United States

Tom Archer
Partner,
PwC US
thomas.archer@pwc.com

Arup Chatterji
Partner,
PwC US
arup.Chatterji@pwc.com

Scott Almassy
Partner,
PwC US
scott.d.almassy@pwc.com

Japan

Kimihiko Uchimura
Partner,
PwC Japan
kimihiko.uchimura@pwc.com

Koichi Banno
Partner,
PwC Japan
koichi.banno@pwc.com

Taiwan

Jacky Lu
Partner,
PwC Taiwan
jacky.l.lu@pwc.com

About PwC Semiconductor Center of Excellence (CoE)

PwC Semiconductor CoE is a specialized global team of semiconductor experienced professionals within the PwC Global Network, covering key territories including Korea, Germany, the US, Japan, and beyond. The PwC Semiconductor CoE is committed to delivering innovative solutions and insights to address the challenges faced by clients across the semiconductor ecosystem.

For more details about the report, please contact the **PwC Semiconductor CoE**

Disclaimer